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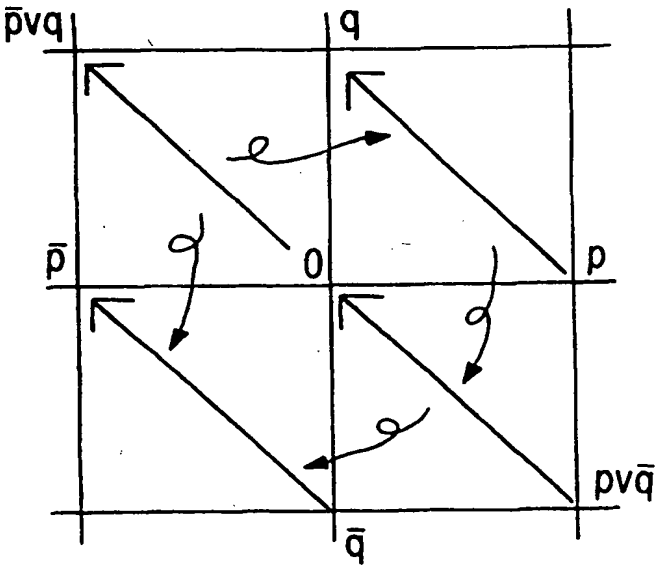
(54) Title: DEVICES AND TECHNIQUES FOR LOGICAL PROCESSING

(57) Abstract

The invention is directed to apparatus, methods, systems and computer program products which permit a simplification of the logic required for performing a certain function to a minimum set of logical elements of operations, permitting a complex digital circuitry to be simplified so that the processing speed for performing the complex digital operations, is reduced. This is accomplished by using a system of propositional logic (13B), representing the logic of a logical circuit to be designed as points and vectors in a vector space, simplifying the logic of the logical circuit to a simpler form using the points and vectors in a vector space, and designing the circuit using the simpler form.



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DEVICES AND TECHNIQUES FOR LOGICAL PROCESSING

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates to the field of logical processing and, more particularly to devices and techniques for simplifying digital logic.

Description of related art

Logic can be described as techniques and operations by which one moves from what one knows to be true to new truths. The principles of logic have been applied in the design and operation of digital logic circuits. Modern-day computers and other processing devices have utilized digital logic extensively. Many of the problems to which digital logic can be applied are complex, involving many independent variables. This results in extremely complex logical circuits in which large numbers of operations are performed. The cost associated with manufacturing and fabrication of such complex digital circuits is great. It would be highly desirable to reduce the number of complements required for performing a particular logical function or set of functions while at the same time increasing the speed with which those functions can be performed.

Digital computers are, of course, well-known. More recently, optical computers have been developed which can perform logical functions using optical elements. These optical computers can perform the same functions performed by digital computers but in principle much faster.

SUMMARY OF THE INVENTION

The invention is directed to apparatus, methods, systems and computer program products which permit a simplification of the logic required for performing a certain function to a minimum set of logical elements of operations. The this permits the complexity of digital circuitry to be simplified the processing speed with which complex digital operations can be performed, reduced.

This is accomplished using a system of propositional logic in which propositions are represented as vectors or displacement in a space. This is applied to the simplification problem, the problem of finding a method for reducing logical schema to a shortest

equivalent. Applications of these techniques to the problems of electrical circuit minimization, to free-space optical processing, to flat optical processing, and to logical processing using color imagery are described.

BRIEF DESCRIPTION OF DRAWINGS

The objects, features and advantages of the system of the present invention will be apparent from the following description in which:

Figure 1 represents two-dimensional space for propositions.

Figure 2 illustrates the propositions p and $p \vee q$ in the space of figure 1.

Figure 3 is a diagram of the vector two-dimensional space showing in the conditional normal schemata or CNS-plane.

Figure 4 is a diagram of the vector two-dimensional space showing the alternational normal schemata or the ANS- plane.

Figure 5 is a diagram showing modus ponens in the CNS-plane.

Figure 6 is a diagram showing modus tollens in the CNS- plane

Figure 7 use a diagram showing the disjunctive syllogism in the CNS- plane.

Figure 8 is the diagram showing how the ANS- and CNS- planes relate.

Figure 9 is a diagram illustrating operations within the ANS- space.

Figure 10 shows an extension of the ANS- plane of Figure 4 to a three-dimensional ANS-space.

Figure 11 shows an extension of the CNS- space to three dimensions together with a hypothetical syllogism.

Figure 12A illustrates a hypothetical syllogism with three variables in the CNS- space.

Figure 12B shows a view of the hypothetical syllogism in the three-dimensional CNS-space.

Figure 13A illustrates a cancellation technique used in simplifying logical representations and in accordance with the invention.

Figure 13B shows the representations of Figure 13A in graphical form.

Figure 13C illustrates implication and equivalence.

Figures 14 A, 14B and 14C illustrate a solution to the simplification problem using the techniques of the invention.

Figure 15 shows a 4-clause schema simplified.

Figure 16A shows a 3-clause schema simplified.

Figure 16B shows the truth-table for the representation of Figure 16A.

Figure 17 shows a 4-variable vector diagram simplification.

Figure 18A is a diagram illustrating the Fix Rule for d = 2.

Figure 18B is an illustration of an example of the Fix Rule.

Figure 19 is an illustration of the Fix Rule for d = 3.

Figure 20 illustrates application of the invention to situations in which developed normal formulas are not the point of departure.

Figure 21 illustrates the equivalence of a developed alternational formal and its undeveloped counterpart.

Figure 22 illustrates the simplification of an undeveloped set of statements.

Figure 23 illustrates another simplification of an undeveloped set of statement taken from Quine.

Figure 24 illustrates an equivalence within the set of statements shown in Figure 23.

Figure 24A illustrates superfluity in the Consensus Theorem and its dual in the CNS-form in a truth-table.

Figure 25 illustrates the Consensus Theorem.

Figure 26 illustrates the dual of the Consensus Theorem.

Figure 27 illustrates a superfluity shown in Figure 23.

Figure 28 illustrates a target circuit to be simplified in accordance with the invention.

Figure 29 shows a simplest circuit equivalent to the target circuit.

Figure 30 is an illustration of optical computation of modus ponens.

Figure 31 is an illustration of interferometric processing for modus ponens to the

Figure 32 illustrates an optical element used for disconjunction and conjunction in a free-space optical processing.

Figure 33 is an illustration of flat optical processing.

Figure 34 or is an illustration of vector addition utilizing sequences of spatial light modifiers.

Figure 35 is an illustration of colorimetric computation of modus ponens.

Figure 36 is a colorimetric simplification of $\mathbf{pq \vee p\bar{q}}$.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Part I of this paper describes a system of propositional logic in which propositions are represented as vectors or displacements in a space. Part II gives the application of the system to the simplification problem, the problem of finding a method for reducing a truth-functional schemata in alternational normal form to a shortest equivalent. Part III is about applications: (i) to problems of electrical circuit minimization; (ii) to free-space optical processing; (iii) to "flat" optical processing; and (iv) to logical processing using colorimetry.

Part I

Imagine a space in which the co-ordinates from the origin **0** are propositional addresses or *possibilities*. Let (1, 0) be the propositional address **p**, and (0,1) the propositional address **q**. Then (1, 1) is the point **p, q**, and we can let the sign "+" be an operation on **p** and **q** which is defined by distance and direction from the origin, by which '**p+q + p+q**' is an instruction to go two units in a **p**-ward direction, and two units in a **q**-ward direction. The operation performed by someone obeying this instruction is commutative and associative.

We can now represent the *proposition* that **p** as a directed line-segment or vector along the **p**- or **x**-axis from the origin **O** to the point or propositional address p in the space, representing the vector **p** in boldface as is standardly done to distinguish it from the possibility p which is represented as the point at the arrowhead of **p**. We can also let the vector **q** be the proposition **q**, represented in the space as the vector pointing straight up the **q**- or **y**-axis to the point q.

Now if we build up the space interpreting the operation "+" as "**v**", the **x**- and **y**-axes will obviously represent lines of logical equivalence. At (2, 0), or **p, p**, for example, we will find the arrowhead of **p v p**, and at (3, 0) the arrowhead of **p v p v p**. These and the rest of the proposition vectors along the **p**-axis are logically equivalent to the base

vector **p**. At (0, 2), or **q**, **q**, we will find the arrowhead of **q** v **q**. Thus **p** and **q** will stand in for the usual unit vectors **i** and **j**. (The vector space of propositions can however have infinitely many directions such as **s**, **t**, **u**, **v**..., which will become important later on when a technique is given to simplify propositions with large numbers of literals.)

We are also now in a position to represent the proposition **p** v **q** in the space as **p** + **q**, the vector resultant of the vectors **p** and **q**, which travels from the origin to **p**, **q**. Then **p** v **q** is itself a vector.

I will call a vector diagram for the propositional calculus such as Figure 2 a **V-Diagram** for the proposition or schema. ("V" is for vector, which is from the Latin word meaning "carrier", "traveller" or " rider".) The V-diagram can be further built up by adding the negation symbols for the negative vectors $\bar{p}$ and $\bar{q}$ in the negative or reverse directions along their respective axes. So we arrive at all of the literals, which are single letters and negations of single letters, and we can also find pairs of single negated or unnegated letters, the propositions **p** v $\bar{q}$, and $\bar{p}$ v $\bar{q}$.

Let us call the vector two-space in Figure 3 the CNS-plane for the plane of the "conjunctional normal schemata".

We are now free to explore another plane, the plane of the alternational normal schemata, or the ANS-plane as I shall call it, in which the points are not alternations but conjunctions, and the vector operation "+" within the space is interpreted as alternation. The ANS-plane and the CNS-plane are duals, so that each point in each plane correspond to its dual in the other plane. This also means that the uniting operation in the CNS-plane is related to the dual of the operation in the ANS-plane, and *vice versa*. In the CNS-plane "+" is alternation, and so in the ANS-plane it is conjunction. The operation "→" in "α→ β" in the CNS-plane is to be read as implication or the assertion of the conditional. In the ANS-plane "→" is to be read as the denial of the *negation* of implication, which is the denial of the conjunction of the antecedent with the negation of the consequent. The whole ANS-plane is to be read as a systematic set of denials, the denials that the propositions given at the base of the vector arrowheads imply a contradiction. This will

be obvious if we remember that arrows *ending* at the origin rather than those issuing from it, as in the CNS-plane, are assertions in the ANS-plane.

In both of the planes certain familiar truths appear as expressions of the main principle which governs "+" or vector addition, the so-called parallelogram law of Galileo. In the CNS-plane we can think of the premises of an argument as component vectors, and the resultant as the conclusion. Then an elementary valid argument–form in the CNS-plane is a parallelogram starting at the origin **O** in that plane. The conjunction of the alternations yields the conclusion, and we get modus ponens appearing as in Diagram 5. If the vectors are represented as displacements around **O** in the **V**-diagram, the modus ponens in the CNS-plane is the set of displacements

	p	**q**		
Premise 1	-1	1	+	$\bar{p}$ **v q**
Premise 2	1	0		**p**
Conclusion=	0	1		**q**

Modus tollens appears as:

	p	**q**		
Premise 1	-1	1	+	$\bar{p}$ **vq**
Premise 2	0	-1		$\bar{q}$
Conclusion=	-1	0		$\bar{p}$

The disjunctive syllogism appears, with its displacement matrix, as:

	p	q		
Premise 1	1	1	+	p v q
Premise 2	0	-1		$\bar{p}$
Conclusion=	0	1		q

Consider now the relation between the CNS-plane and the ANS-plane. There clearly is one, as they share the literals and the all-important origin **0**. The two planes can be brought into harmony if we represent them, arbitrarily, as lying above and below the origin in a space whose third dimension runs along the conjunction-alternation axis, putting alternation at the top and conjunction at the bottom.

The result is a space, or the part of it near **0**, with two planes above and below the origin. The origin **0** appears in the vertical axis between the two planes. The whole space of Figure 8 generates further principles of the propositional calculus. Take **p v q** in the top right hand corner. Negating it comprehensively, in all three dimensions, or developing it through the origin, gives the point $\bar{p}\,\bar{q}$ in the ANS-plane. This is one of the two forms of DeMorgan's theorem. Its other form can be found by comprehensively negating **pq** in the ANS-plane, and travelling through **0** to $\bar{p}$ **v** $\bar{q}$ in the CNS-plane. The CNS-/ANS-space as a whole has an intriguing and beautiful structure, as it combines the dimensions of alternation and conjunction, the various propositions formed from atomic **p** and **q**, and the dimension of negation.

Operations within the ANS-space have "+" representing conjunction. When all the non-equivalent conjunction points are established in the space, pairs and other combinations of the given points or conjunctions are given as alternations or vectors. So

we get a resultant of **pp** from **pq** v **p**$\bar{q}$ by relating the two vectors to the origin **0** in a parallelogram (Figure 9).

In the CNS-space, on the other hand, the corresponding operation produces alternations, and the operation within the space which combines them is conjunction. So we get sets of conjunctions, e.g. those important ones involving $\bar{p}$ **v q**, which are among the more important *arguments* of natural deduction.

Assume now in the ANS-space a third proposition **r**, and a third dimension **z** in which the unit vector **r** is to be found. So we get the **r**-plane, the one swept out by the vector **r**. This space can also be represented in two dimensions on the page. In Figure 10 the negation-affirmation axis, which follows the **z**-axis in the order of rotation of the variables about **0**, is inserted to prevent the occlusion of lines and points.

To check the validity of the hypothetical syllogism (-1, 1, 0) (0, -1, 1), (-1, 0, 1), with three variables, in the CNS-space, we can represent it as in Figure 11.

The validity of the argument appears, using three sets of coordinates, as

	p	**q**	**r**		
Premise 1	-1	1	0	+	$\bar{p}$ **v q**
Premise 2	0	-1	1		$\bar{q}$ **v r**
Conclusion =	-1	0	1		$\bar{p}$ **v r**

Note the simplicity of the given representation or perspective on the hypothetical syllogism in Figure 11, matched only by the simplicity of the **pqr** string –1, 1, 0, 0, 1-, 1, -1, 0 1, which is merely a set of instructions for displacements in a 3-space.

The vector system can be used in the CNS-space to display other principles, for example implications, by which $\bar{p}$ v **q** implies **p**→**q**. It also shows that $\bar{p}$ v **q** implies **0** →. $\bar{p}$ v **q**, as well as $\bar{q} \rightarrow \bar{p}$ and $\bar{p}$ v $\bar{q}$ →**0**. Furthermore, the vector system shows nicely the principle of material equivalence, which states that (**p**→**q**)(**q**→**p**) is equivalent to **p**↔**q** (Figure 13).

The starting point of all these vectors, together with the direction, gives the end point. "Together with" here means treating the points and directions algebraically as themselves directions from the origin. This yields a cancellation technique in which a starting-point of **0** is cancellation of no literal, and an end point of **0** is the cancellation of all the literals

Starting Point	Direction	End Point
0	$\bar{p}$ v **q**	$\bar{p}$ v **q**
p	$\bar{p}$ v **q**	**q**
$\bar{q}$	$\bar{p}$ v **q**	$\bar{p}$
p v $\bar{q}$	$\bar{p}$ v **q**	**0**

Parallel principles can be given for the ANS-plane. Here "α→β" means the same as in the CNS-plane; which is α⊃β, the conditional, but the reason is hard to see, though interesting. Take the proposition **p** → **q** in the CNS-plane. It is represented by (among others) an arrow from the point **p** to the point **q**. In the ANS-plane we find an arrow from **p** to **q**. Call it **v**. But what does **v** mean? Note that the CNS-plane vector from **p** to **q** is true if **v** is false. For **v** is **p** $\bar{q}$, and the same vector or direction as **p** $\bar{q}$ → **0**. If we want the ANS-plane vectors to represent truth, we must read them as the *denials* of the conjunction of the proposition **p** at the base of the arrow with the negation of the proposition **q** at the arrowhead, or –(**p** $\bar{q}$). Each arrow in the ANS-plane then reliably represents a conditional.

This reveals something further about the all-important $\underline{0}$, the origin. We have just learned that in the ANS-plane an arrow from **p** to **q** is $p\bar{q}$, to be read however as a negation. So what does $\alpha \rightarrow \mathbf{O}$ mean? **O** is $p\bar{p}$. So the conjunction of α and $-(\mathbf{O})$ of α-(**pp**). But this is $\alpha(\bar{p} \vee p)$, which is equivalent to α.

Similarly, in the CNS-plane, all the arrows which depart from **0** represent an instance of $\alpha \vee ß$, where α is **O**. Take an arrow from **O** to **p v q**. **O** is the tautology $p \vee \bar{p}$. The negation of this $p\bar{p}$, and so the arrow to the point **p v q** is $-(p \vee \bar{p}) \vee pq$. But the first disjunct of this is equivalent to $p\bar{p}$, and so it is always false. Hence the alternation is equivalent to the second disjunct, or the assertion **pq**.

If a vector in the ANS-space is directed towards **O**, **O** has the effect of reversing the truth-values of the base propositions. Moving towards **O** from the base (**p**,**q**) in the CNS-space we get the vector $\bar{p} \vee \bar{q}$. **O** has the effect of putting **p** and **q** through the Sheffer-function "|". The vector moving *away from* **O** in the CNS-space *towards* e.g. (**p**,**q**) is also the vector from the base (**p**,**q**) to **O**, and so it is the vector $\bar{\bar{p}} \vee \bar{\bar{q}}$ or **p v q**.

In a dual fashion, if we are moving *towards* **O** in the ANS-space, we get the base values, so that **pq**→**O** is **pq**. From **O**, a vector to $(\bar{p},\bar{q})$ will thus be **pq**. In the ANS-space **O** has the effect of putting **p** and **q** through the dagger function "↓", by which **p**↓**q** is $\bar{p}\bar{q}$.[1]

[1]Wittgenstein's operator N in the *Tractatus* could be described as a generalization of ↓ to more than two places, as N(p,q,r), for example, is **pqr**. We could also describe a generalized Sheffer operation for more than two places which trANS-forms a base such as say (**p**,**q**,**r**,**s**) into **p v q v r v s**. This operation could be called S for "Sheffer".

Part II

The simplification problem is the problem of reducing truth-functional schemata (or, in the system I am describing, systems of vectors in the ANS-space) to their shortest equivalents. A practical method for doing this, in alternational normal form continues, as Quine observes (Quine, 1982, p. 78), to be suprisingly elusive.

In the ANS-space "vector logic" can be applied to the problem in the following way. Take the schema **pq v p$\bar{q}$**, which as well as implying **p** is equivalent to **p**. To simplify it, form the parallelogram from the origin **0**, **pq** and **p$\bar{q}$** to the resultant or vector sum point. Call it **i**, for "implicant". The vector acting at **i**, which is in this case **pp**, implies **pq v p$\bar{q}$**. So **i** splits up alternationally, into its components, **pq v p$\bar{q}$**, towards the origin.

Next note that **pq** is equivalent to **pqp**, so that the arrowhead at **pq** can be dragged to **pqp**. But **pp** can also be dragged to **p**. Now we have an arrow from **p to pqp**. But this arrow an be translated into a position on top of the arrow from **p$\bar{q}$** to **pp**. The same procedure yields a double-headed arrow between **pq** and **pp**, and the result can be read as **pq v p$\bar{q}$ ↔ p**.

When an implicant splits up into its alternations towards the origin, if there is a proposition **σ** (for "simplest equivalent") at the center of the parallelogram formed by **0**, the disjuncts of a two-clause target schema, and **i**, then **σ** is a shortest equivalent of the target schema. But this only works for pairs of schemata which do have an **i**-point.

The general simplification procedure, in the ANS-space, is as follows.

(1) Represent the alternational normal schema, the target schema **t**, as a set of vectors in the ANS-space. Each clause or disjunct of **t** is a position vector (i.e. one pointing to **O**) with **O** at one corner of a parallelogram made of propositional addresses to the **i**-point at the other . Any two other outside vertices of such a parallelogram are implicants which are among the original clauses of **t**.

(2) Pick any two clauses. If there is a propositional address σ at the midpoint between the component clauses, the vector from **i** to σ, i.e. σ, is the simplification of and can replace the relevant clauses of **t**, as in the case where **t** is **pq v p**$\bar{q}$, **i** is **pp** and σ is **p**.

(3) Generate i-implicants until each clause or vector has been used at least once. If a disjunct **d** of **t** cannot be used because it forms no propositional address with any other disjunct, then **d** must appear unmodified in the final schema which is the simplification of **t**.

(4) If an i-point exists in **t**, delete the vectors which produce it in favor of the vector from **i** to **O**.

(5) For a clause in a schema which subsumes another clause, e.g. **pqr v pq**, eliminate the subsuming clause, in this case **pqr**, leaving **pq**. Implications arising from subsumption can be written into the whole vector system of **t** as components where relevant. For example, an arrow can be drawn from **pqr** to **pq** in the above example.

Rule (5) applies for example to **pq v p**, which is an undeveloped or unbalanced schema in which **pq** subsumes **p**. How does **pq v p** simplify to **p**, when it seems to yield **p v q**? The Answer, which cashes the metaphor of "subsumption", is that **p** really represents a plane, in a 3-space, sweeping out the whole **p**-domain, or any ANS-schema with **p** in it. So it is a kind of type fallacy to represent **pq** alongside **p** in a single schema as if they were to be treated separately. For **pq**, and **p**$\bar{q}$, are really "elements" of **p** itself. A cube is not so many faces and so many lines, but it can be represented as lines producing faces or vice versa. As a matter of philosophy, therefore, vector logic can avail itself, as rule (5) does, of a preliminary use on Quine's operation (i) from "A Way to Simplify Truth Functions", which has us 'drop the subsuming clause ... if one of the clauses of alternation subsumes another...'. Quine's operation (i) also replaces $\alpha \vee \bar{\alpha} \phi$ with $\alpha \vee \phi$, and the same for the corresponding α -schemata (Quine, 1955, p. 627).

(6) Couples such as **pq v** $\bar{p}\bar{q}$ or $\bar{p}\bar{q}$**s v pq**$\bar{s}$ cannot be summed to zero, the origin.

(7) Translate vectors as in Figure 14. Any superpositions of parallel arrows in opposite directions represent equivalences. (a) Drop the longer clause at the end of any double-headed arrow. (b) Drop pairs, triples etc. of double-headed arrows which meet at a point in favor of the vector from that point to **0**. (c) Drop a vector or clause in the target schema which is itself the resultant of any other two vectors.

(8) A simplification is complete if in the system which replaces the target schema: (a) no vectors or clauses are subsumed by others (see Rule 5); (b) no double-headed vectors remain, or, in other words, if all equivalences in the system have been exploited.

Take next the simplification of the four-clause target schema $\mathbf{pqr} \vee \mathbf{pq}\bar{r} \vee \bar{p}\mathbf{qr} \vee \mathbf{p}\bar{q}\bar{r}$. The first job is to plot the target schema in a V-diagram. We get two parallelograms, with two i-points, **qrqr** and $\mathbf{p}\bar{r}\,\mathbf{p}\bar{r}$, and two σ-points, **qr** and $\mathbf{p}\bar{r}$, which are final in the sense that they do not generate a further σ-point. Hence the target schema is equivalent to $\mathbf{qr} \vee \mathbf{p}\bar{r}$.

Now take the simple-looking three-clause schema $\mathbf{pqr} \vee \mathbf{pq}\bar{r} \vee \mathbf{p}\bar{q}\bar{r}$. The resultant is $\mathbf{pq} \vee \mathbf{p}\bar{r}$.

Here the σ- and i- points function as before. But something else has happened. The vector $\mathbf{pq}\bar{r}$ has been used twice, once along with **pqr** to give **pq**, and again, with $\mathbf{p}\bar{q}\bar{r}$, to give $\mathbf{p}\bar{r}$. Why was $\mathbf{pq}\bar{r}$ not exhausted by its first use, and why can it be used again? The Answer can be seen by looking at the truth-table for $\mathbf{pqr} \vee \mathbf{pq}\bar{r} \vee \mathbf{p}\bar{q}\bar{r}$, which is

1. **pqr** T
2. $\mathbf{pq}\bar{r}$ T
3. $\mathbf{p}\bar{q}\mathbf{r}$
4. $\mathbf{p}\bar{q}\bar{r}$ T
5. $\bar{p}\mathbf{qr}$

6. $p\mathbf{q}\bar{r}$
7. $\bar{p}\,\bar{q}\mathbf{r}$
8. $\bar{p}\,\overline{qr}$

Truth, it could be said, is not exhausted by use. The $\mathbf{p}\bar{r}$ of line 2 is so to speak redundant, as line 2 has already been captured by the disjunct **pq**, and so line 4 has had half of its work already done.

This simplification procedure is theoretically an improvement on the techniques used in Karnaugh maps (Garrod and Borns, 1991, p. 153 ff.), as it needs no wrapping around and can be used mechanically and easily on more than four variables – any number fits into the "proposition circuit", which gradually turns from a square, with two variables, into a hexagon, with three, and finally into a circle, with an infinite number of variables. With four variables, the logical space is as given in Figure 17.

The whole figure in Figure 17 is a "measure polytope" or hypercube, though one with a further complex internal structure. There is no limitation of tessellation to the number of propositional variables or vectors **p, q, r s** ... that can be handled, because the space is derived not from a closed figure, such as a cube, but from a sheaf of lines in the geometrical sense. Not all closed figures tessellate. All the lines of the multi-dimensional sheaves are coincident.

Consider in Figure 17 a simplification from $pqr\bar{s}$ v $pq\bar{r}\bar{s}$ v $pq\bar{r}s$ v $\bar{p}qr\bar{s}$ v $p\bar{q}\bar{r}s$ v $\bar{p}q\bar{r}\bar{s}$ to $p\bar{r}s$ v $q\bar{s}$. This proceeds as shown, with the six vectors reducing to two. The first vector or σ-point in the simplification, $p\bar{r}s$, results from the implicand pair $pq\bar{r}s$ v $p\bar{q}rs$, dropping the up-down $q/\bar{q}$ component. In this case we have a simplification from two four-letter schemata to one three-letter schema. The remaining four schemata are all needed to fix the σ-point $q\bar{s}$. Both pairs $pqr\bar{s}$ v $p\bar{q}\bar{r}s$ and $pq\bar{r}\bar{s}$ v $\bar{p}qr\bar{s}$ must give a fix on the same σ-point if the reduction from four literals to two is to be justified. For either pair by themselves is not sufficient for the required biconditional. The general rule is

$$V=2d$$

where v is the number of vectors required to make the fix on the σ-point, and d is the drop in the number of literals from the clauses of the given schema to the resulting clause in the target schema.

Another illustration of the Fix Rule is pqr v $pq\bar{r}$ v $p\bar{q}r$ v $p\bar{q}\bar{r}$ v $\bar{p}qr$ v $\bar{p}q\bar{r}$ v $\bar{p}\bar{q}r$, which is , however, equivalent merely to p v q v r, as it covers every line of the truth-table except $\overline{pqr}$.

One pair of implicands is $p\bar{q}r$ v $pq\bar{r}$, which give the σ-point p. But as this is a drop down from three letters to one, we need a fix of four vectors or two vector sums on the point, and the third and fourth vectors $\bar{p}qr$ and $pq\bar{r}$ provide it. The same sort of fix appears with q (pqr v $\bar{p}q\bar{r}$ and $\bar{p}qr$ v $pq\bar{r}$) and r ($\bar{p}\bar{q}r$ v pqr and $\bar{p}qr$ v $p\bar{q}r$).

A much simpler though negative example of the Fix Rule is $\mathbf{pq}\bar{r}\ \mathbf{v}\ \mathbf{p}\bar{q}\ \bar{r}$, which seems to give **p** as an σ-point resultant, but fails to for lack of a fix on the point **p**, as four, not two vectors must converge on it for the drop. This acts as a constraint on the vector arithmetic. We seem to get

	p	q	r	
	1	1	1	+
	1	-1	-1	
=	1	0	0	.

But the Fix Rule rules this out. If x columns are filled with numbers, positive or negative, then the number of non-zero columns in the sum must be **x-1**. The Fix Rule will seem entirely unartificial when one recognizes that what it means in, say, a 3-space, is that a literal or one-letter proposition is a *face*, and so four corners are needed to determine it. A two-letter proposition is a *line*, and so only two letters are needed to fix it. And a point in a 3-space is a three-letter proposition.

Consider as another illustration of the Fix Rule $\mathbf{pqrs}\ \mathbf{v}\ \mathbf{pqr}\bar{s}\ \mathbf{v}\ \mathbf{pq}\bar{r}\mathbf{s}\ \mathbf{v}\ \mathbf{pq}\bar{r}\ \bar{s}\ \mathbf{v}\ \mathbf{p}\bar{q}\mathbf{rs}\ \mathbf{v}\ \mathbf{p}\bar{q}\mathbf{r}\bar{s}\ \mathbf{v}\ \mathbf{p}\bar{q}\bar{r}\mathbf{s}\ \mathbf{v}\ \mathbf{p}\bar{q}\bar{r}\ \bar{s}$. This is very obviously equivalent to **p**, and since d = 3 for each clause, **v** for the point **p** = 2d. So **d** = 8, and eight vectors or four vector sums are needed for the fix on the σ-point.

In many cases the target schema is unbalanced in the sense that its clauses have different numbers of conjuncts and so they need to be put into developed alternational normal form. An example $\mathbf{pq}\ \mathbf{v}\ \mathbf{p}\bar{q}\mathbf{r}\ \mathbf{v}\ \bar{p}\ \bar{q}\ \bar{r}$ (Quine, 1982, p. 75). This is equivalent to $\mathbf{pq}\ \mathbf{v}\ \mathbf{pr}\ \mathbf{v}\ \bar{p}\ \bar{q}\ \bar{r}$. Like the early Quine's procedure in "The Problem of Simplifying Truth Functions" (Quine, 1952, p. 524), the vector simplification method given so far has taken the cumbersome 'developed normal formulas as the point of departure.'

If **t** is developed uniformly we get $\bar{p}\,\bar{q}\,\bar{r}$ v **p**$\bar{q}$**r** v **pqr** v **pq**$\bar{r}$ **r**, which in a V-diagram is clearly $\bar{p}\,\bar{q}\,\bar{r}$ v **pq** v **pr**, as **pr** lies midway between **pqr** and **0**, and **pq** lies midway between **pqr** and **pq**$\bar{r}$. But without development, we can take the iota-point for **p**$\bar{q}$**r** v **pq**, which is **pr**, and argue that since **pr** →.**p**$\bar{q}$**r** v **pq** (where ".expression" and "expression." represents bracketing of the "expression" that precedes or follows the dots), and **pr** subsumes **p**$\bar{q}$**r**, the longer **p**$\bar{q}$**r** can simply be replaced by its own implicant.

The equivalence of undeveloped

(i) $\bar{p}$**q** v **p**$\bar{q}$ v $\bar{q}$**r** v **q**$\bar{r}$

and

(ii) **p**$\bar{q}$ v $\bar{p}$**r** v **q**$\bar{r}$

is harder to establish. It is one which resists as many as twelve fell swoops (Quine, 1982, p. 76, also in 1952, pp. 523-527) or shorter truth-tables. In the vector space with developed alternational forms the equivalence is easy enough to see. The developed form of this equivalence is easy enough to see. The developed form of this example is: $\bar{p}$**qr** v $\bar{p}\,\bar{q}$**r** v $\bar{p}$**q**$\bar{r}$ v **pq**$\bar{r}$ v **p**$\bar{q}\,\bar{r}$ v **p**$\bar{q}$**r**.

The same result can be obtained using column matrices for the pairs of vectors. Then for $\bar{p}$**qr** v $\bar{p}\,\bar{q}$**r** we get

p	**q**	**r**		
-1	1	1	+	$\bar{p}$**qr**
-1	-1	1		$\bar{p}\,\bar{q}$**r**
-1	0	1		$\bar{p}$**r**

And for $\bar{p}q\bar{r}$ v $pq\bar{r}$ we get

	p	q	r		
	-1	1	-1	+	$\bar{p}q\bar{r}$
	1	1	-1		$pq\bar{r}$
=	0	1	-1		$q\bar{r}$

Similarly, for $p\bar{q}r$ v $p\bar{q}\bar{r}$ we get

	p	q	r		
	1	-1	1	+	$p\bar{q}r$
	1	-1	-1		$p\bar{q}\bar{r}$
=	1	-1	0		$p\bar{q}$

It should be noted that in this example too the Fix Rule applies. It would be nice to take the vectors in a different order, so that $p\bar{q}r$ and $pq\bar{r}$ are chosen instead of $p\bar{q}r$ and $p\bar{q}\bar{r}$, and also $\bar{p}q\bar{r}$ and $p\bar{q}\bar{r}$ instead of $\bar{p}q\bar{r}$ and $pq\bar{r}$. This would yield r and p instead of pq and $q\bar{r}$ in the whole system. But that would mean dropping from three letters to one in the case of these two pairs of alternations, and we cannot do that as there is no fix on r or on p.

There may of course be more than one "shortest" schema. In Quine's example there is obviously is on inspection a second. The vector system $\bar{q}r$ v $\bar{p}q$ v $p\bar{r}$ has the same overall "effect" in the vector-logical space.

Let us now try this example with the use of the i-points, the key prime implicants. Take first $\bar{p}q$ v $\bar{q}r$. This alternation is implied by the i-vector which forms the parallelogram with 0. But there is no Φ-point, and so, apparently, $\bar{p}q$ v $\bar{q}r$ is not

equivalent to $\bar{p}\,\mathbf{r}$. Yet in the context of the whole scheme $\mathbf{p}\bar{q}\ \mathbf{v}\ \bar{q}\,\mathbf{r}\ \mathbf{v}\ \bar{p}\,\mathbf{q}\ \mathbf{v}\ \mathbf{q}\bar{r}$, it is. To see this, we move the free vectors $\mathbf{p}\bar{q}$ and $\mathbf{q}\bar{r}$ from the right-hand side of the V-diagram to the parallelogram on the left. The implicand of $\mathbf{p}\bar{r}$, which is $\mathbf{p}\bar{q}\ \mathbf{v}\ \mathbf{q}\bar{r}$, slides into place from $\mathbf{p}\bar{q}\ \mathbf{v}\ \mathbf{q}\bar{r}$ back to $\bar{p}\,\mathbf{r}$, and the two-way implication or equivalence is established.

The vector summation of $\mathbf{p}\bar{q}$ and $\bar{q}\,\mathbf{r}$ to $\mathbf{p}\overline{qq}\,\mathbf{r}$ or $\mathbf{p}\bar{q}\,\mathbf{r}$ is disallowed by the Fix Rule, according to which the number of vectors needed to make a fix is equal to the d-th power of 2. This summation would actually produce a negative value for d. As the number of literals rises from two to three, the drop *increases* from 2 to 3, or –1.

Quine gives another interesting example of a simplification with four simplest equivalents, one which also illustrates the method of simplification for non-developed or unbalanced schemata like the last example. The example (Quine, 1952, p. 528) is $\mathbf{pqr}\ \mathbf{v}\ \mathbf{p}\bar{r}\ \mathbf{v}\ \mathbf{pq}\bar{s}\ \mathbf{v}\ \bar{p}\,\mathbf{r}\ \mathbf{v}\ \bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$ (Figure 23).

We begin by generating vector sums for the various disjuncts. We can see fairly easily that $\bar{p}\,\mathbf{r}$ and $\bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$ to start with, yield a parallelogram, but it seems to end at an **i**-point outside the logical space. Yet if we study that point, we can see that it is actually at the co-ordinates $\bar{p}\,\bar{q}\,\bar{r}\,\bar{s}\,\bar{p}\,\mathbf{r}$. This point, however, contains a contradictory or backward *and* forward instruction, namely the **r** from $\bar{p}\,\mathbf{r}$ and the $\bar{r}$ from $\bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$ which can both be deleted. There is also a double **p** in the final address, and one **p** of these, but not both, can of course be deleted. This leaves an end-point for a vector $\bar{p}\,\bar{q}\,\bar{s}$. By similar reasoning, we can arrive at the vector $\bar{q}\,\bar{r}\,\bar{s}$ as the vector sum of $\mathbf{p}\bar{r}$ and $\bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$. And similarly **pqr** with $\mathbf{p}\bar{r}$ gives **pq**, or **pqr** with $\bar{p}\,\mathbf{r}$ gives the **i**-point **qr**. Each vector must be used at least once if it is not to appear unchanged in the simplified schema.

The corresponding Φ-points, however, do not appear at the designated addresses which are shortened versions of their **i**-points, and so the equivalence of the **i**-points and

their implicands is not established. Just as in the example shown in Figure 20, the drag-back effects described in connection with **p** and **pp** in Figure 14 do not apply.

As before, in Figure 24, we first write in the parallelogram from **0** for the pair **pqr** v $\mathbf{p}\bar{r}$. This gives an L-point at **pqp**, and so from **pqp** we write in a pair of vectors to **pqr** and $\mathbf{p}\bar{r}$. Now **pqr** implies **pq**, and is subsumed by it, and we can represent the subsumption rule here by drawing in the vector from **pqr** to **pqp**. Figure 24 is now showing an *equivalence* between **pqr** and **pq**, but *only in the presence of the* $p\bar{r}$ *in the alternational schema* $pqr \vee p\bar{r}$, i.e. with the translated or "borrowed" vector $\mathbf{p}\bar{r} \rightarrow \mathbf{0}$.

It is worth realizing that in the reductions in developed normal form, the implicands can be replaced by the implicant only because of the various biconditionals or double arrows at work. There is no intrinsic magic in the Φ-point. In the undeveloped examples, too, clauses do not disappear in a general way because pairs of disjuncts collapse into their implicants, but because of the presence of specific conditions elsewhere in the schema, which translated have the effect or creating biconditionals.

Finally, why is $\mathbf{pq}\bar{s}$ superfluous in the example given in Figure 23? The Answer is interesting and complicated, and principles about superfluity need to be established.

Take the truth, sometimes known as the Consensus Theorem, that **pq v** $\mathbf{p}\bar{r}$ **v qr.** $\leftrightarrow$**.pq v** $\bar{p}$ **r.** Representing this in the ANS-space for **p**, **q** and **r**, we can see that the implicant **qr** is the resultant of the disjunction of **pq** and $\bar{p}$ **r** (Figure 25). We can give it as a general truth that implicants, in the ANS-space, are resultants.

Let the left-hand side of the Consensus Theorem be represented as

qp v $\bar{p}$ **r v qr**

The Theorem says that the disjunct **qr** is superfluous. Consider the dual of the left-hand side of the Theorem, in the CNS-space. It is

$$(q \vee p)(\bar{p} \vee r)(q \vee r)$$

This is the conjunction ($\bar{q}$ p)(p r)($\bar{q}$ r). But clearly the last conjunct is superfluous, as the first two conjuncts imply it by a hypothetical syllogism, in the sense that if they are true, so is it (Figure 25).

It is nice to see the dual roles of conjunction and alternation, or ANS-and CNS-spaces, truth and falsehood, and how the concept of the *resultant* and the *component* binds them together.

In the following truth-table, we can that the (q r) resultant is so to speak "covered" by its component with respect to truth, in the ANS-space, and falsity in the CNS-space. That is, with the disjunctions in the ANS-space the addition of an extra truth on already true lines of the truth-table does not affect the truth of the whole schema. And similarly in the CNS-space, if the whole schema is already false, adding a false conjunct will not affect that result.

			ANS-				CNS-	
p	q	r	qr	v	pq	v $\bar{p}$ r	(q v p)	(p v r)	(q v r)
T	T	T	T		T			F	
T	T	F			T				
T	F	T							
T	F	F						F	F
F	T	T	T			T			
F	T	F							
F	F	T				T	F		
F	F	F					F		F

We are now in a position to deal with the superfluity of **pq** $\bar{s}$ in Quine's example in Figure 24. Disjunctive clauses in the ANS-space like **pq** $\bar{s}$ are superfluous when they are components. Before the representation of the schema **pqr v** $\bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$ **v p** $\bar{r}$ **v** $\bar{p}$ **r v pq** $\bar{s}$ with a view to simplification, we can simply run a check to see if any of the clauses are implicants or iota-points for any others. We can easily find that **pq** $\bar{s}$ **→ .pqr v p** $\bar{r}$ from the truth-table for the schema; all the lines on which **pq** $\bar{s}$ is true are also lines on which either **pqr** or **p** $\bar{r}$ is already true, and so **pq** $\bar{s}$ can be deleted from the schema to be simplified.

Geometrically, the construction is as follows: (Figure 27). Note that **pq** $\bar{s}$ extends to **pq** $\bar{s}$ **p**. This is however the implicant for **pqr** $\bar{s}$ **v p** $\bar{r}$. However, **pqr** $\bar{s}$ itself extends to **pqr** $\bar{s}$ **pq**. This last schema is the implicant for **pqr v pq** $\bar{s}$. So **pq** $\bar{s}$ gives way to **p** $\bar{r}$ **v pqr** $\bar{s}$. But **pqr** $\bar{s}$ can itself can be dropped in favor of **pqr v pqr** $\bar{s}$. Any line of the

truth-table for **pqr** on which is true is also one which either **pqr** or $\mathbf{p}\bar{r}$ is already true. Hence $\mathbf{pq}\bar{s}$ can be dropped.

So for Quine's example in Figure 23 we are left with the four possibilities:

These examples, and others like them, suggest the possibility of further applications of simplifying geometrical theorems and methods to the simplification problem.

The charm of a vector simplification technique is that is follows a least-action principle, for any number of propositional vectors, in the sense that the problem is not one of finding shortest equivalents to truth-functional schemata. Rather the space, inasmuch as it is fixed vector space in which all free vectors having the same direction are in a sense the *same* directional vector, is unable *not* to give the desired result.

As to propositional logic as whole, it is nice to have all of the nineteen or however many clanking "rules of inference" within the space, so that there is just the one intuitively obvious method of argument: vector addition. It is really absurd to think of empty or "formal" rules such as association and communication as having the same status as say modus tollens, which is genuine "motor" that advances arguments through logical space. Association and commutation should flow out of the nature of the logical space, and in the vector space they do. The vectors **p v q** and **q v p**, for example, have the same end-point, though they arrive at it by different but corresponding routes.

Part III

(i) Electrical and Integrated Circuit Minimization

Let us now see how the techniques described can be used in a routine for simplifying electrical and integrated circuits. Take the target circuit $\mathbf{ABC} + \mathbf{A}\bar{C} + \mathbf{AB}\bar{D} + \bar{A}\mathbf{C} + \bar{A}\,\bar{B}\,\bar{C}\,\bar{D}$ (Figure 28).

The first job is to plot this in the ANS-space as the set of vectors $\mathbf{pqr}\ \mathbf{v}\ \mathbf{p}\bar{r}\ \mathbf{v}\ \mathbf{pq}\bar{s}\ \mathbf{v}\ \bar{p}\mathbf{r}\ \mathbf{v}\ \bar{p}\,\bar{q}\,\bar{r}\,\bar{s}$, as in Figure 23 above. Following the routine (1)-(8) given on p. 20, above, we can simplify this system of vectors to e.g., $\mathbf{pq}\ \mathbf{v}\ \bar{p}\mathbf{r}\ \mathbf{v}\ \mathbf{pr}\ \mathbf{v}\ \bar{p}\,\bar{q}\,\bar{s}$ (cf. p. 39).

The resultant schema can then be translated into the circuit diagram $AB + A\overline{C} + \overline{A}C + \overline{A}\,\overline{B}\,\overline{D}$ (Figure 29).

Note that the target circuit has five gates (G=5), that the total number of inputs into these gates is twelve (I=12), and that the redundancy factor (i.e., the number of times an original input is used again, corresponding to the join dots) is seven (R=7). These figures drop to G=4, I=9 and, most importantly, R=2 for the simpler circuit, representing corresponding gains in materials savings, speed and reliability.

(ii) Free Space Optical Computation

More than ten years ago the National Academy of Sciences Panel on Photonics Science and Technology Assessment declared that 'The ultimate benefit of photonic processing could occur if practical optical logic could be developed' (Whinnery et. al., *Photonics*, 1988, p. 35). So far the implied challenge of the Panel has not been met.

Vector manipulation has been one of the big success stories for optical computation, but vector techniques themselves promise an application to the logic of optical computation as a whole. The full ANS-/CNS- space could be built as an optical device for checking the validity of arguments or as a logic device for optical computation, and also as simplification machine. Each operation in the space is a laser, and the resultant proposition-points such as **p** and **pq** and **pqr** are multifaceted beamsplitters or mirrors which reflect the beams in the correct logical directions at the correct logical strengths to ensure the required implications.

Thus in Figure 30 a beam **V** can be sent from the origin to a half-darkening beamsplitting mirror at the node p. At p it is split and sent at half-strength to q, and to $\overline{q}$. Simultaneously, a second beam **U** from **O** is sent to the node $\overline{p}$ **v q**, which is also **p→q**. At this point **U** is split and sent at half-strength to $\overline{p}$ and to **q**. The proposition **p** is said to "half-imply" **q**, in the sense that with one other proposition it *does* imply **q**, and the proposition $\overline{p}$ **v q** is said to "half-imply" **q** in the sense that with one other proposition (**p**) it *does* imply **q**.

Both half-implication beams are coincident on **q**, and at **q** the photoreceptor gives a reading of .5 + .5 or 1. The system has optically computed *modus ponens*; from an

input of **p** and an input of $\bar{p}$ **v q**, it has yielded up **q**. The system gives a physical interpretation of beamsplitting as multiple implication and of darkening as fractional implication.

The same principles will apply to the other rules of inference and logical equivalences.

A development of the system given for *modus ponens* in Figure **30** obviates the need for a free beam for e.g., **p** to **q**, and simplifies the design of the node. In Figure **31**, the beam to **p** is split, at full-strength, to **p**'s implicants, which are **p v q** and $\bar{p}$ **v q** (ignoring tautologies). The beamsplitter at $\bar{p}$ v q itself directs the beam to **q** at only half-strength, and the desired computation is achieved.

We can also arrange that in an embodiment of the uninterpreted **(p, q, ... n)** space, in which the base **(p,q)** is either **p v q** or **pq** (though not both), configurations of the beamsplitters will allow the node to switch between the two states. A conjunctional state will correspond to a *concave* configuration, as both inputs are required for the activation of the node, and an alternational state will correspond to a *convex* configuration, as shown in Figure 32.

(iii) "Flat" Optical Processing

A second method of exploiting the vector system for computation is more markedly spatial. Represent the propositions in the uninterpreted **(p,q)** space with spatial light modifiers (SLMs). When the first premise is input, e.g. $\bar{p}$ **v q**, then the origin **0**, and with it the position of the whole space, are moved to the point $\bar{p}$ v q, or in a $\bar{p}$ **v q** direction. We could say the **0** *becomes* $\bar{p}$ **v q**, so that we are now in a $\bar{p}$ **v q** environment, a $\bar{p}$ **v q** world. Then **p** in the second SLM (Figure 33) will *be* **q**, and we have modus ponens. And when the whole space is displaced in a $\bar{p}$ **v q** direction, **q** *is* **p**! The SLMs are shown sequentially in Figure 34.

(iv) Colorimetric Processing

Colored laser beams can be used so that the refractive angle is built into the vector rather than into the propositional nodes as the CIE (Commission Internationale de l' Eclairage) x-y chromaticity diagram (a color mixing diagram) is itself a vector space. (Or a mixed

system of colored laser and colored mirrors could be used.) Then optical computation for simplification is simply the colorimetric process of additive color mixing. IN the CNS-space let **p** be red (R), $\bar{p}$ a complementary cyan blue-green (C), **q** a yellow (Y), $\bar{q}$ a complementary blue (B), **p v q** yellow-red (YR) and $\bar{p}$ **v q** blue-red (BR). Also $\bar{p}$ **v** $\bar{q}$ is the complementary of YR, a cyan blue.

The contradiction of **0** (the so-called "Nullpunkt", or "white") corresponds to the addition of complementary hues.[2] **YR + BR = R**, since **Y** and **B** are complementary.

With these colorimetric assignments we can compute modus ponens and the other rules of argument and truth-preserving substitutions. The proposition **p** is **R**, and **q** is **Y**. So **p→q**, or $\bar{p}$ **v q**, is **CY**. Together with **R** this give **Y** or **q**, as **C** and **R** are complementaries.

In the ANS- space we can perform simplifications colorimetrically. Take the most basic simplification as an illustration, in which **pq v p**$\bar{\mathbf{q}}$ is equivalent to **p**. Let **YR** represent **pq** and **BR p**$\bar{\mathbf{q}}$. The **Y** and **B** beams cancel to the "Nullpunkt", leaving **RR** or **R**, which is **pp** or **p** (Figure 36)

It is still true, as Norbert Streibl et. al. ("Digital Optics", (1989)) pointed out, the 'A uniform technology for digital optical information processing, comparable in its significance to microelectronics, does not yet exist and is by itself a challenging research goal.' A vector logic for optics is a source from which such a "uniform" technology can flow, just as electronics derived from the natural isomorphism of electric circuitry and truth-functional logic.

In this disclosure, there is shown and described only the preferred embodiment of the invention, but, as aforementioned, it is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.

[2] With complementaries '... what is offered, so to speak, in the way of colour by one spectrum (or colour) is withdrawn by the other, so that the result is a vanishing of colour, just as in a contradiction between two propositions which negate one another the result is a vanishing of information' (Jonathan Westphal, *Colour*, Blackwell, 1991, p. 108.

Claims:

1. A method of designing logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit to be designed as points and vectors in a vector space; and
   b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and
   c. designing the logical circuit using the simpler form.

2. A method of manufacturing logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit to be manufactured as points and vectors in a vector space; and
   b. using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form; and
   c. using the simpler form to implement the logical circuit in hardware.

3. A method of simplifying logical circuits, comprising the steps of:
   a. representing the logic of a logical circuit as points and vectors in a vector space; and
   b. modifying the representation in vector space using at least one process rule of a set of process rules to simplify the logic.

4. The method of claim 3 in which at least one process rule of a set of process rules consisting of the following process rules:
   a. Process Rule 1--
      a1. Represent the alternational normal schema, the target schema **t**, as a set of vectors in the ANS-space,

      a2. Each clause or disjunct of **t** is a position vector (i.e. one pointing to **O**) with **O** at one corner of a set of parallelograms made of propositional addresses to the **i**-point at the other,

      a3. Any two other outside vertices of such a parallelogram are implicants which are among the original clauses of **t**;

   b. Process Rule 2--
      b1. Pick any two clauses,
      b2. If there is a propositional address σ at the midpoint between the component clauses, the vector from **i** to σ, i.e. σ, is the simplification of and can replace the relevant clauses of **t**, as in the case where **t** is $pq \vee p\bar{q}$, **i** is **pp** and σ is **p**;
   c. Process Rule 3--
      c1. Generate **i**-implicants until each clause or vector has been used at least once,

c2. If a disjunct **d** of **t** cannot be used because it forms no propositional address with any other disjunct, then **d** must appear unmodified in the final schema which is the simplification of **t**;

d. Process Rule 4--
d1. If an **i**-point exists in **t**, delete the vectors which produce it in favor of the vector from **i** to **O**;

e. Process Rule 5--
e1. For a clause in a schema which subsumes another clause eliminate the subsuming clause;

f. Process Rule 6--

f1. Couples such as $\mathbf{pq} \vee \bar{p}\bar{q}$ or $\bar{p}\bar{q}\mathbf{s} \vee \mathbf{pq}\bar{s}$ cannot be summed to zero; the origin.

g. Process Rule 7--

g1. Translate vectors as in Figure 14 if a corresponding σ-point exist for a **i**-point then 6 is the simplification of **i**.

g2. Any superpositions of parallel arrows in opposite directions represent equivalences,

g3. For equivalences, (a) Drop the longer clause at either end of any double-headed arrow, (b) Drop pairs, triples etc. of double-headed arrows which meet at a point in favor of the vector from that point to **O** and (c) Drop a vector or clause in the target schema which is itself the resultant of any other two vectors;

h. Process rule 8--

h1. A simplification is complete if in the system which replaces the target schema no vectors or clauses are subsumed by others and no double-headed vectors remain (i.e. if all equivalences in the system have been exploited).

5. Apparatus for simplifying logical circuits, comprising:
   a. a processing element configured to represent the logic of a logical circuit to be simplified as points and vectors in a vector space and to use the points and vectors to simplify the logic of the logical circuit to a simpler form.

6. The apparatus of claim 5 in which the processing element is an optical computer.
7. The apparatus of claim 5 in which the processing element is a digital computer.

8. The apparatus of claim 1 in which the processing element is an colorimetric computer.
9. The apparatus of claim 1 in which the processing element is an analog computer.
10. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be designed as points and vectors in a vector space and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form and for designing the logical circuit using the simpler form.

11. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit to be manufactured as points and vectors in a vector space, and for using the points and vectors in a vector space to simplify the logic of the logical circuit to a simpler form, and for using the simpler form to implement the logical circuit in hardware.

12. A computer program product, comprising:
    a. a memory element; and
    b. a computer program stored on said memory medium, said computer program comprising instructions for representing the logic of a logical circuit as points and vectors in a vector space, and for modifying the representation in a vector space using at least one process rule of a set of process rules to simplify the logic.

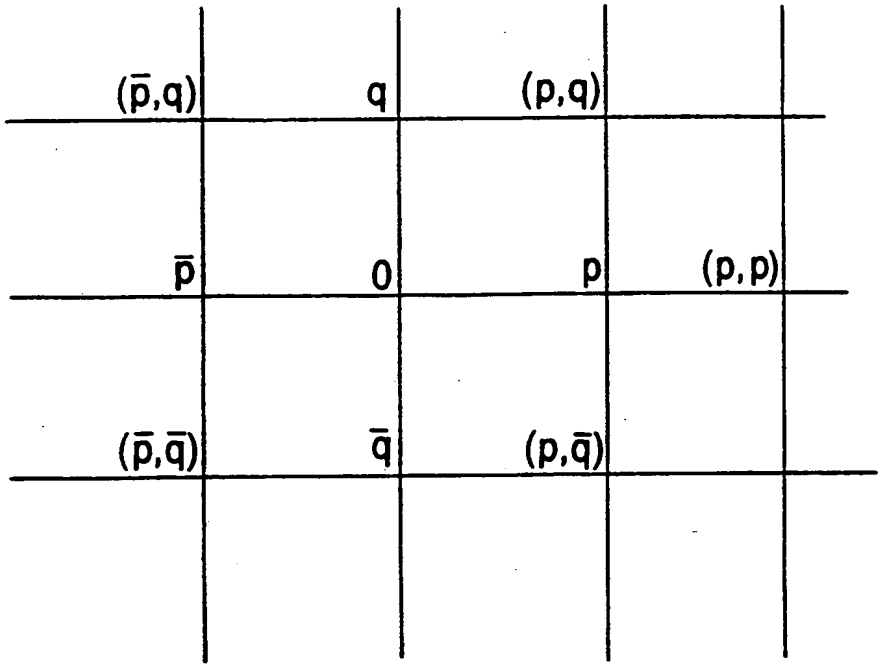


Figure 1
A Space for Propositions

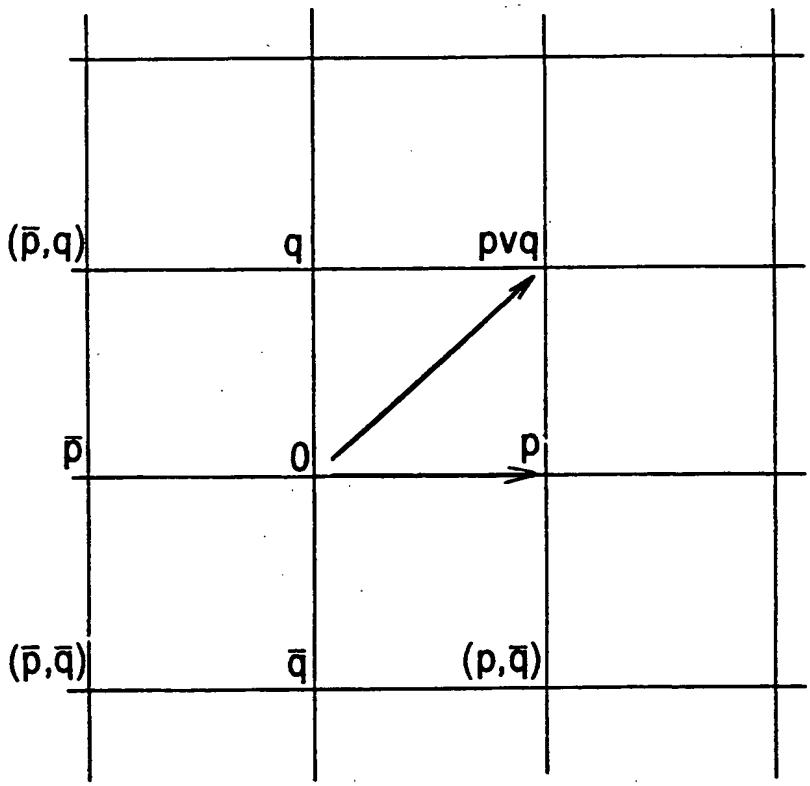


Figure 2

The Propositions p and q v q

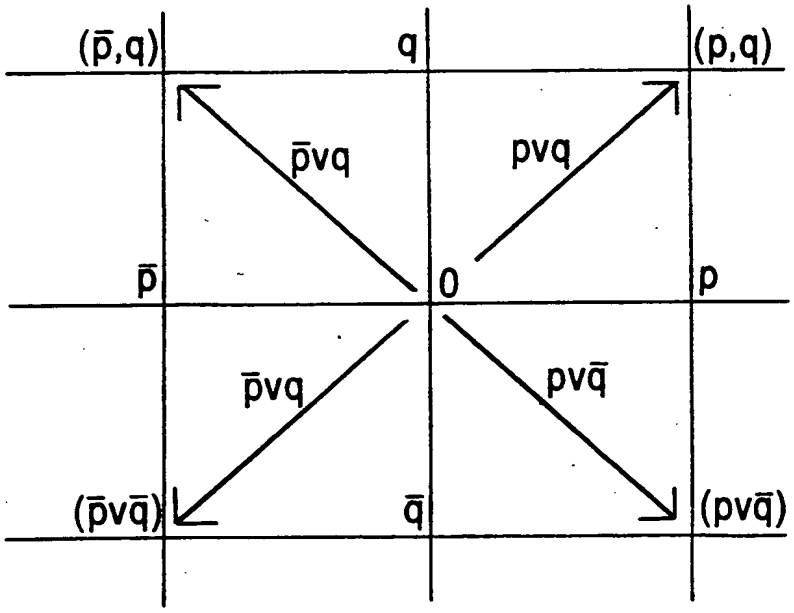


Figure 3

Two-Letter Alternational Clauses

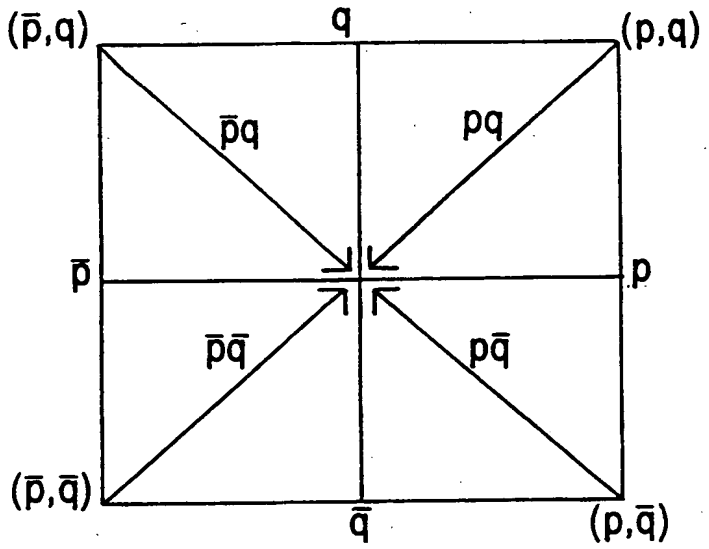


Figure 4

The ANS-plane

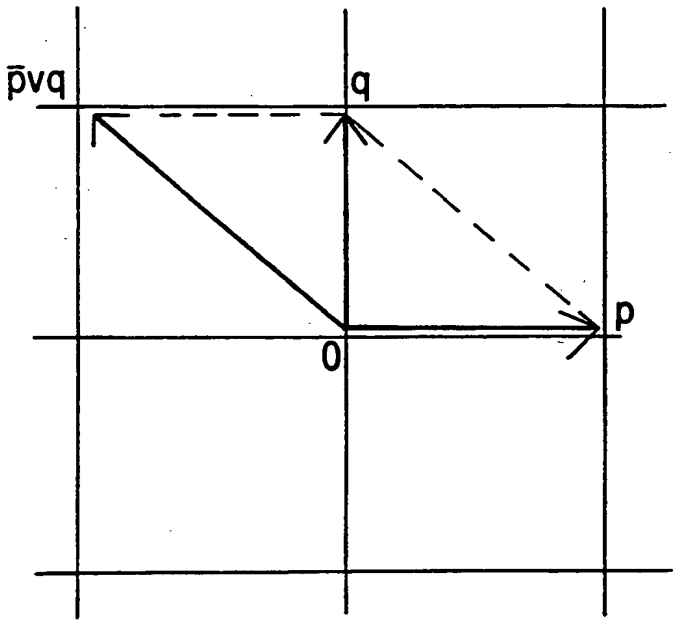


Figure 5
Modus Ponens in the CNS-plane

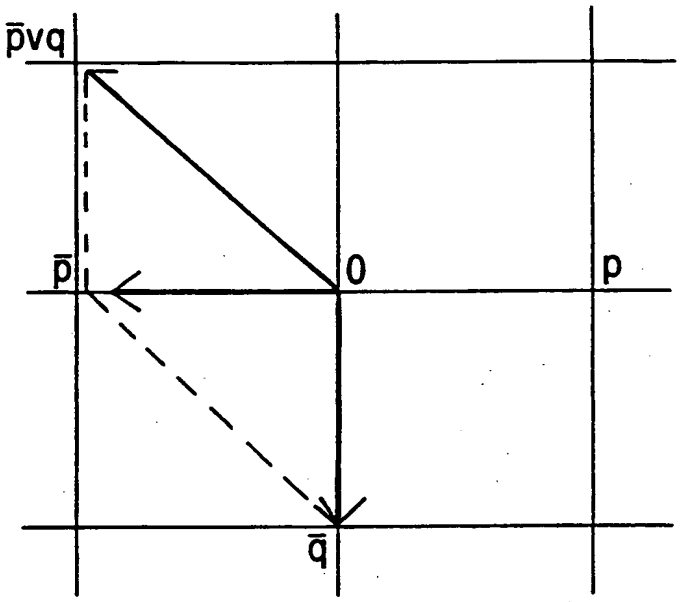


Figure 6
Modus Tollens in the CNS-plane

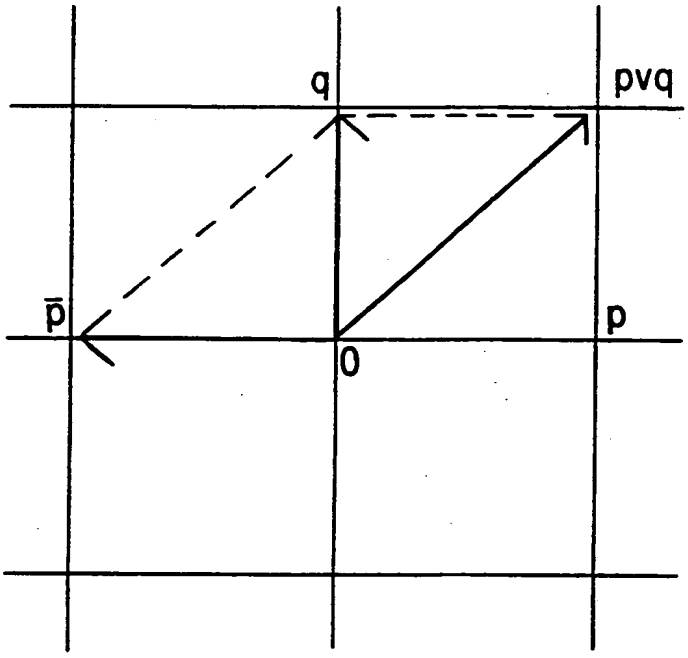


Figure 7
The Disjunctive Syllogism in the CNS-plane

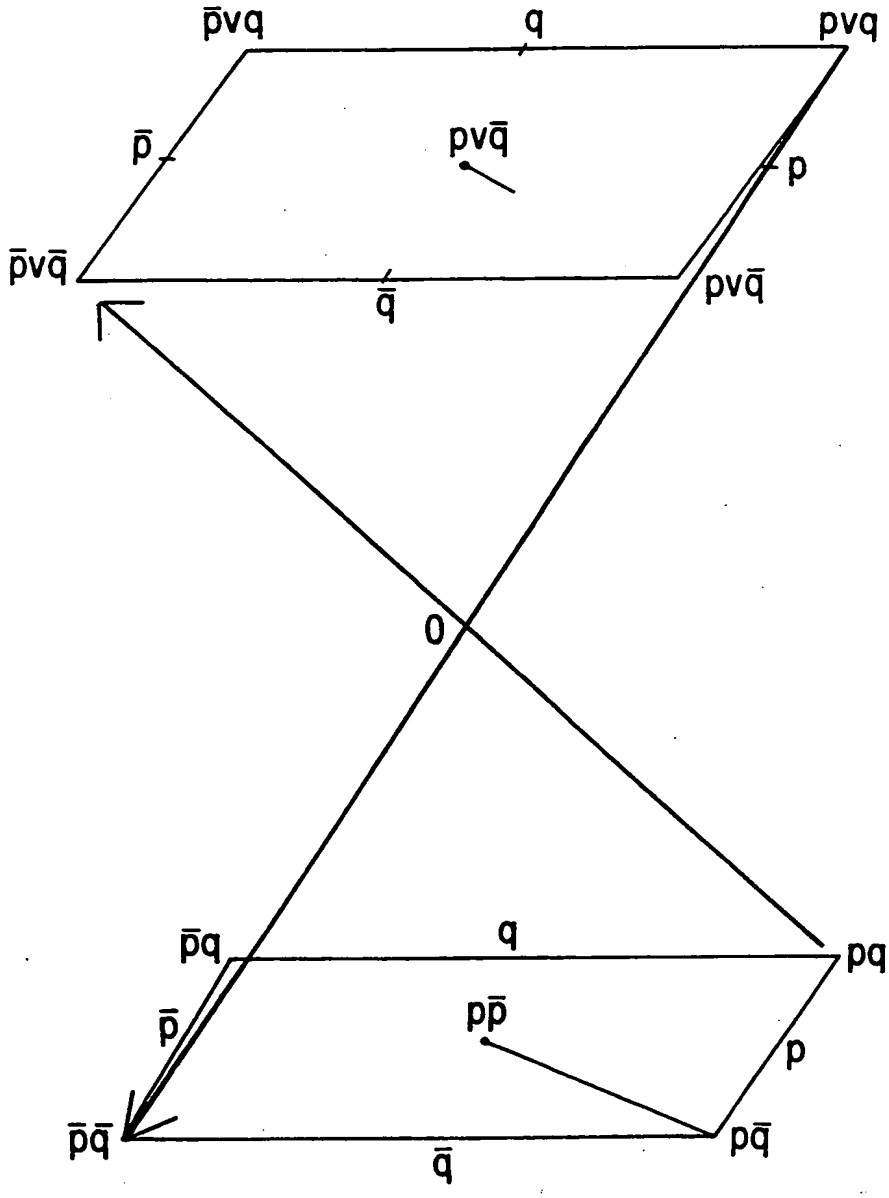


Figure 8

Harmony of ANS-and CNS-planes

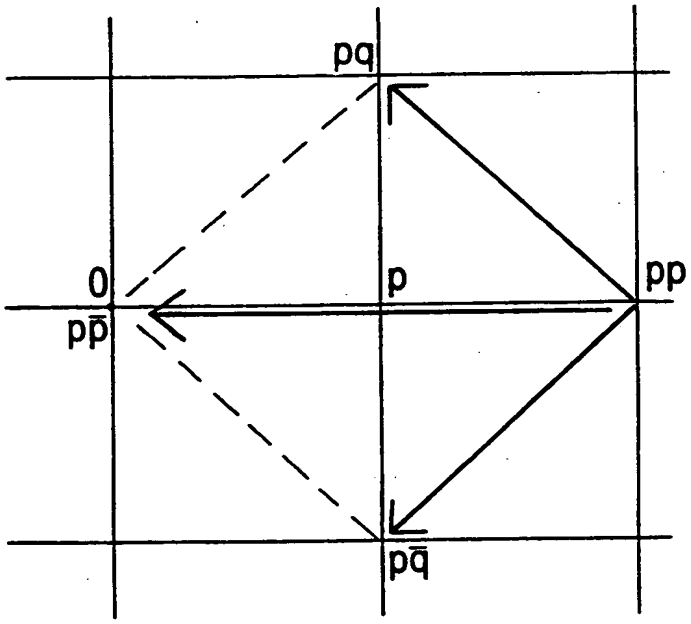


Figure 9

pp +, pq v pq

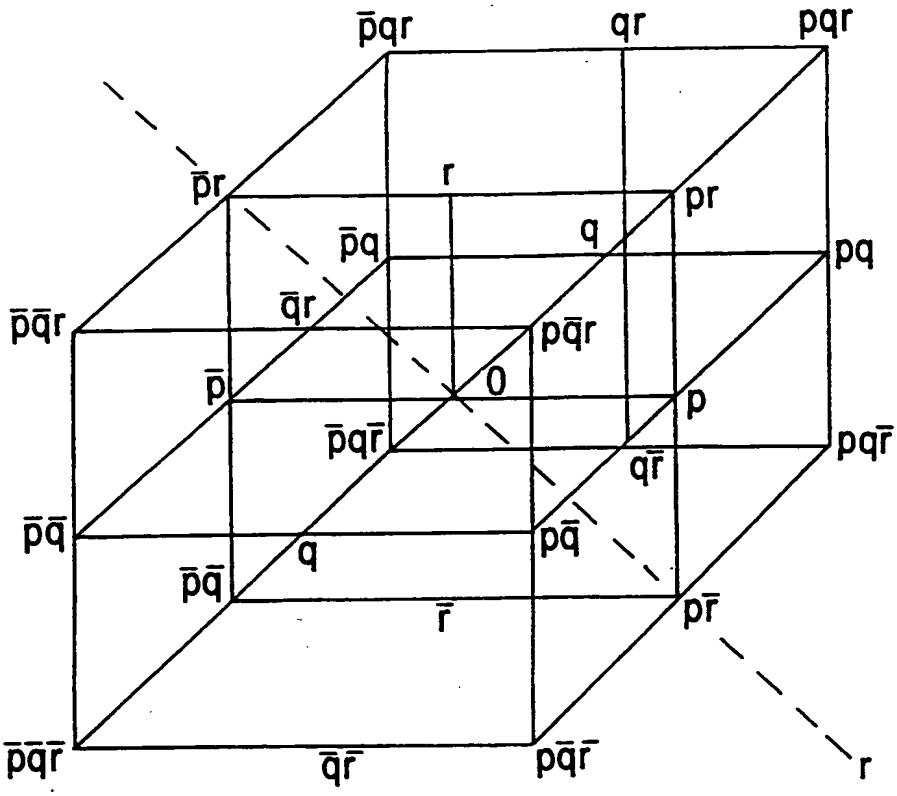


Figure 10

2D Representation of the 3D ANS-Space

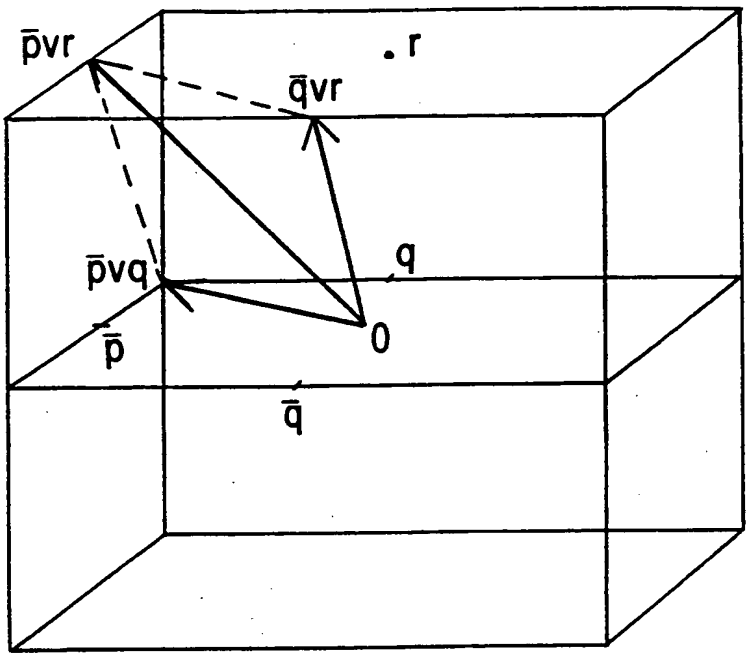


Figure 11
The CNS-space with Three Variables:
the Hypothetical Syllogism

	p	q	r		
Premise 1	-1	1	0	+	$\bar{p}vq$
Premise 2	0	-1	0		$\bar{q}vr$
Conclusion =	-1	0	1		$\bar{p}vr$

Figure 12A

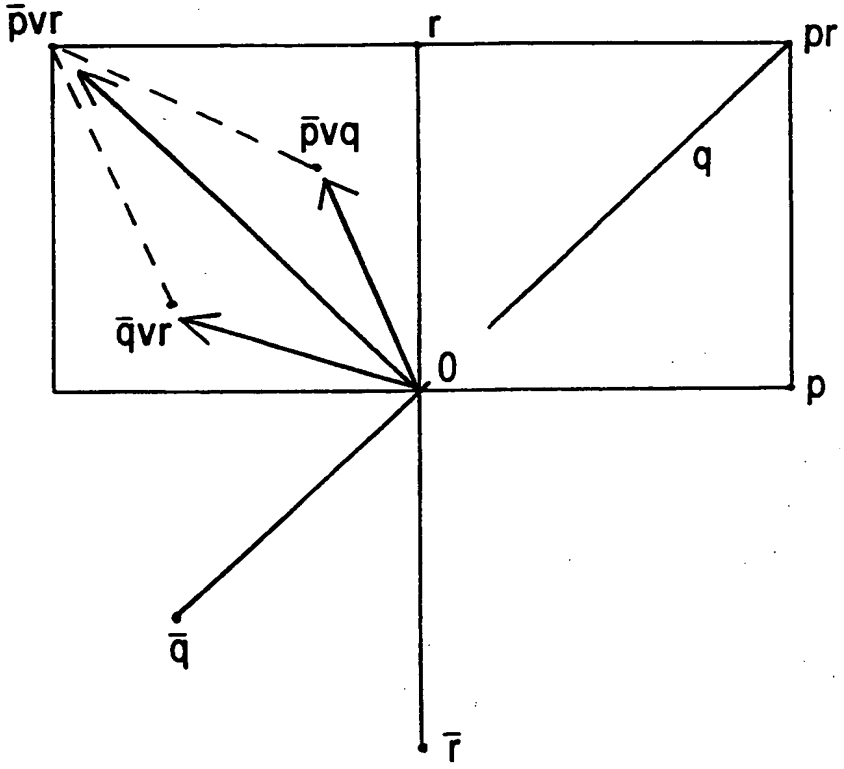


Figure 12B

Hypothetical Syllogism in a 3D CNS-Space

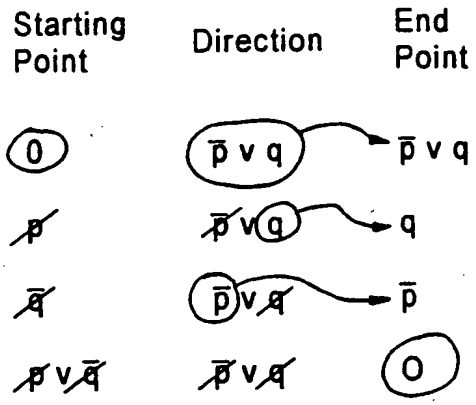


Figure 13A

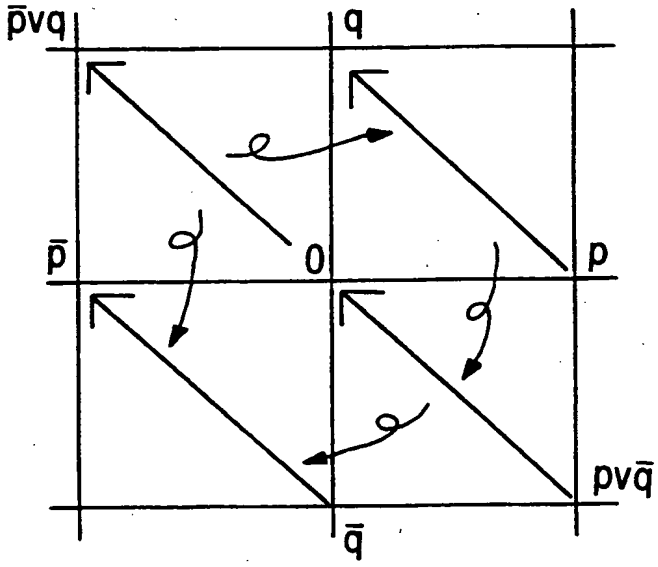


Figure 13B

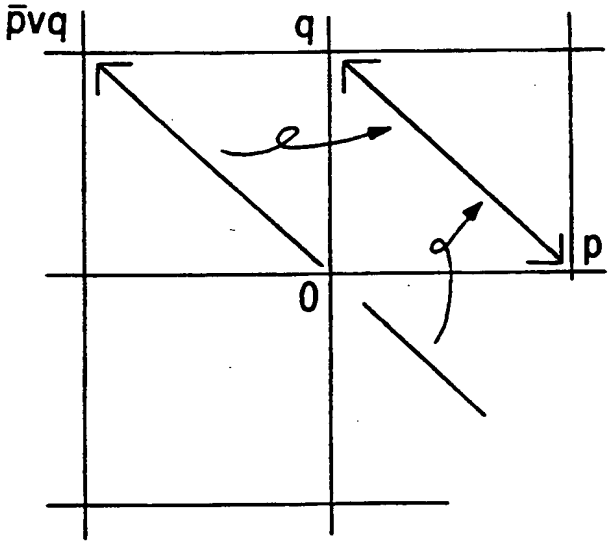


Figure 13C

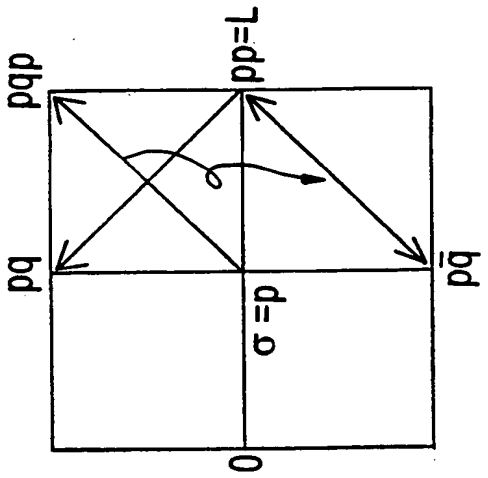


Figure 14C

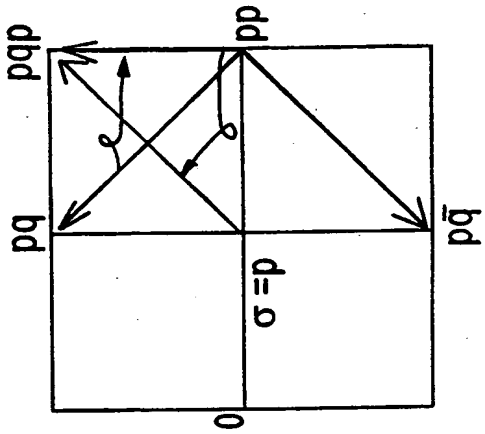


Figure 14B

pq v pq̄ ↔ p

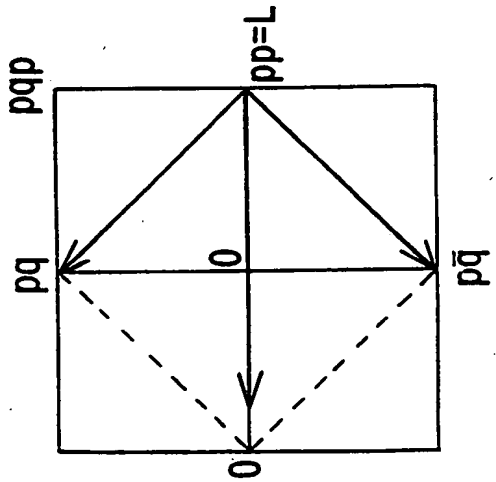


Figure 14A

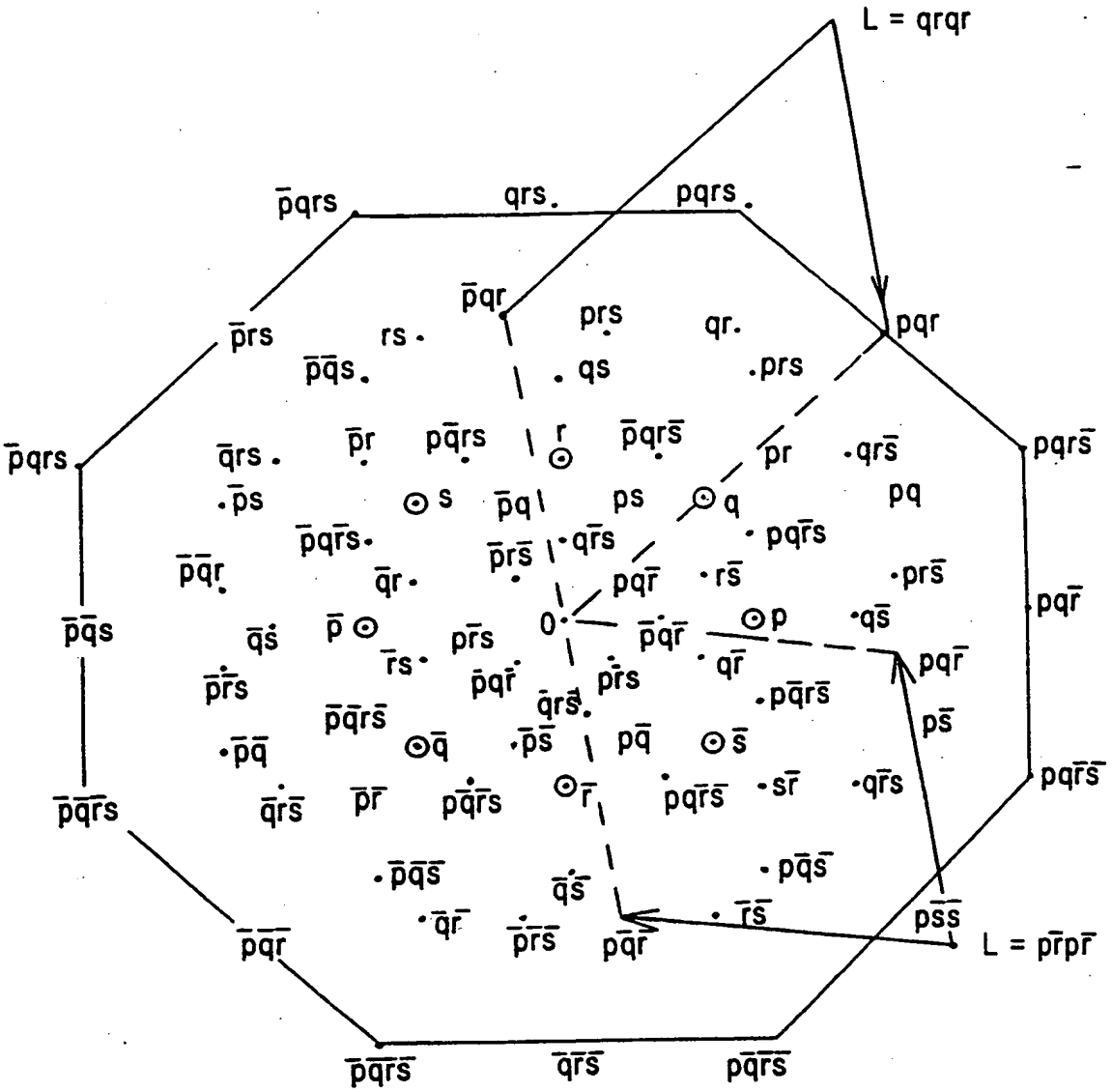


Figure 15

A Four-Clause Schema Simplified

pqr v pqr̄ v p̄qr v p̄q̄r. ◄► .qr v p̄r̄

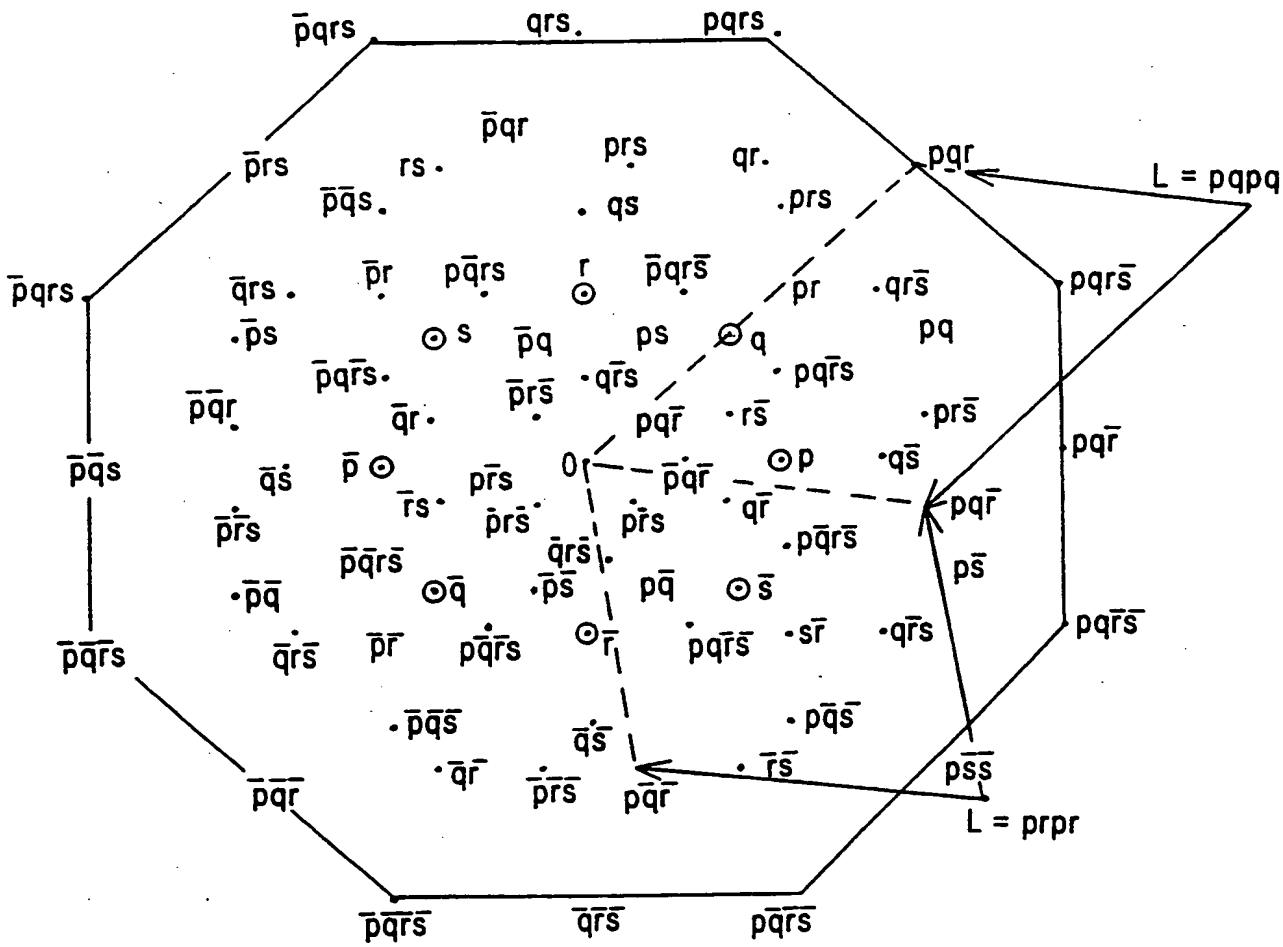


Figure 16A

pqr v pqr̄ v pq̄r̄ v p̄q̄r. ⟷ .qr v p̄r̄

Figure 16B

1.	pqr	T
2.	pqr̄	T
3.	pq̄r	
4.	pq̄r̄	T
5.	p̄qr	
6.	p̄qr̄	
7.	p̄q̄r	
8.	p̄q̄r̄	

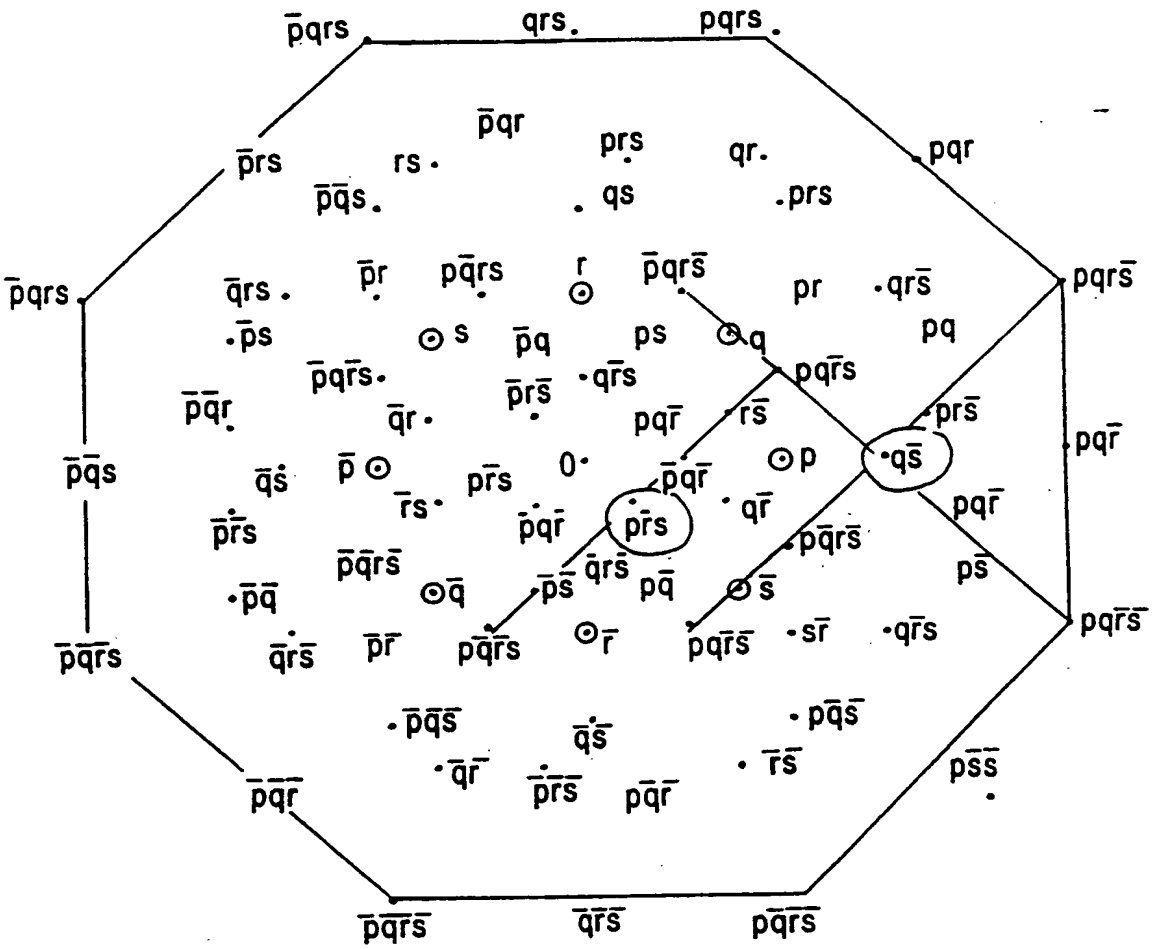


Figure 17

Four-Variable V-diagram with Simplification of
pqrs̄ v pqr̄s v pqr̄s v p̄qrs̄ v p̄q̄rs v p̄qr̄s̄ .... pr̄s v qs̄

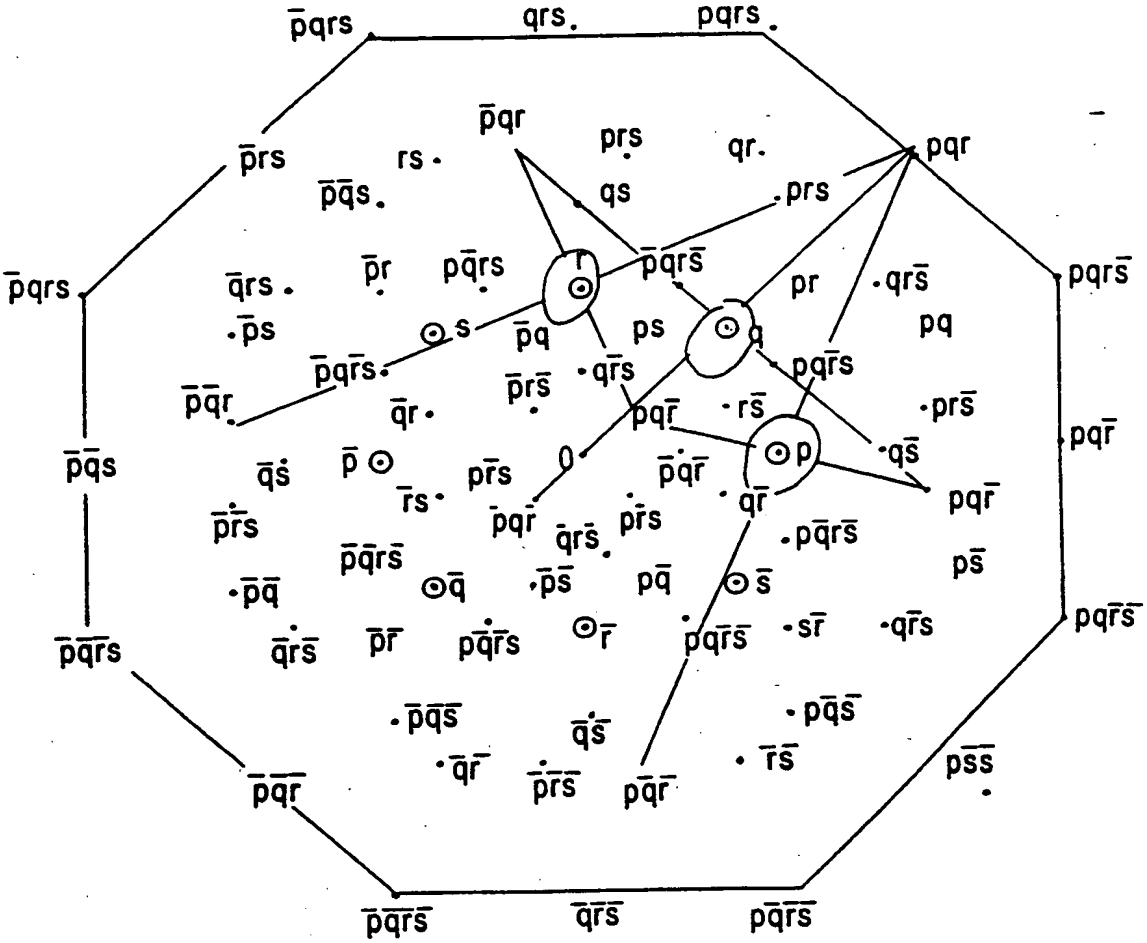


Figure 18A

Fix Rule d = 2

pqr v pqr̄ v pq̄r v pq̄r̄ v p̄qr v p̄qr̄ v p̄q̄r.... p v q v r

p	q	r	
1	1	-1	+
1	-1	-1	
1	0	0	

Figure 18B

p	q	r	
1	1	-1	+
1	-1	1	
1	0	0	

Figure 18C

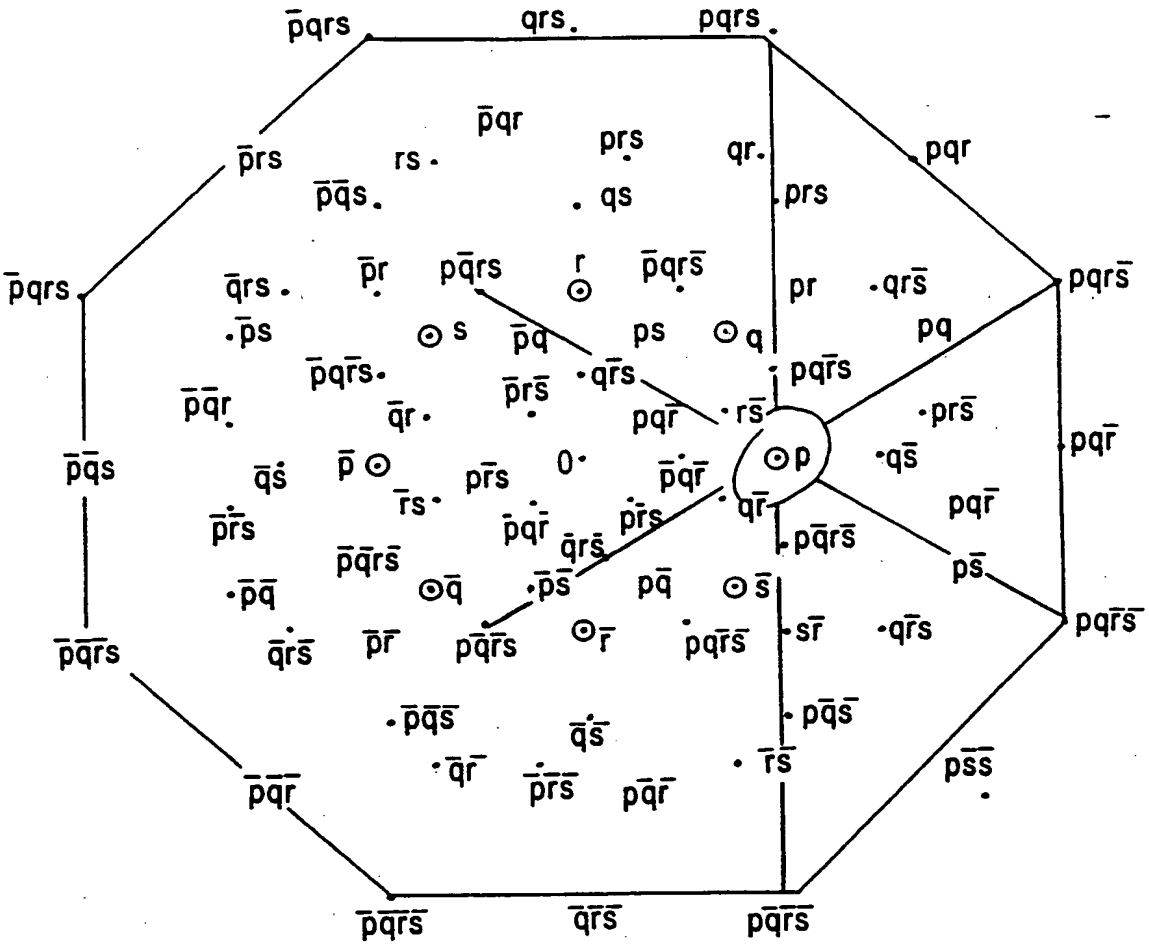


Figure 19

Fix Rule d = 3

pqrs v pqrs̄ v pqr̄s v pqr̄s̄ v pq̄rs v pq̄rs̄ v pq̄r̄s v pq̄r̄s̄. p

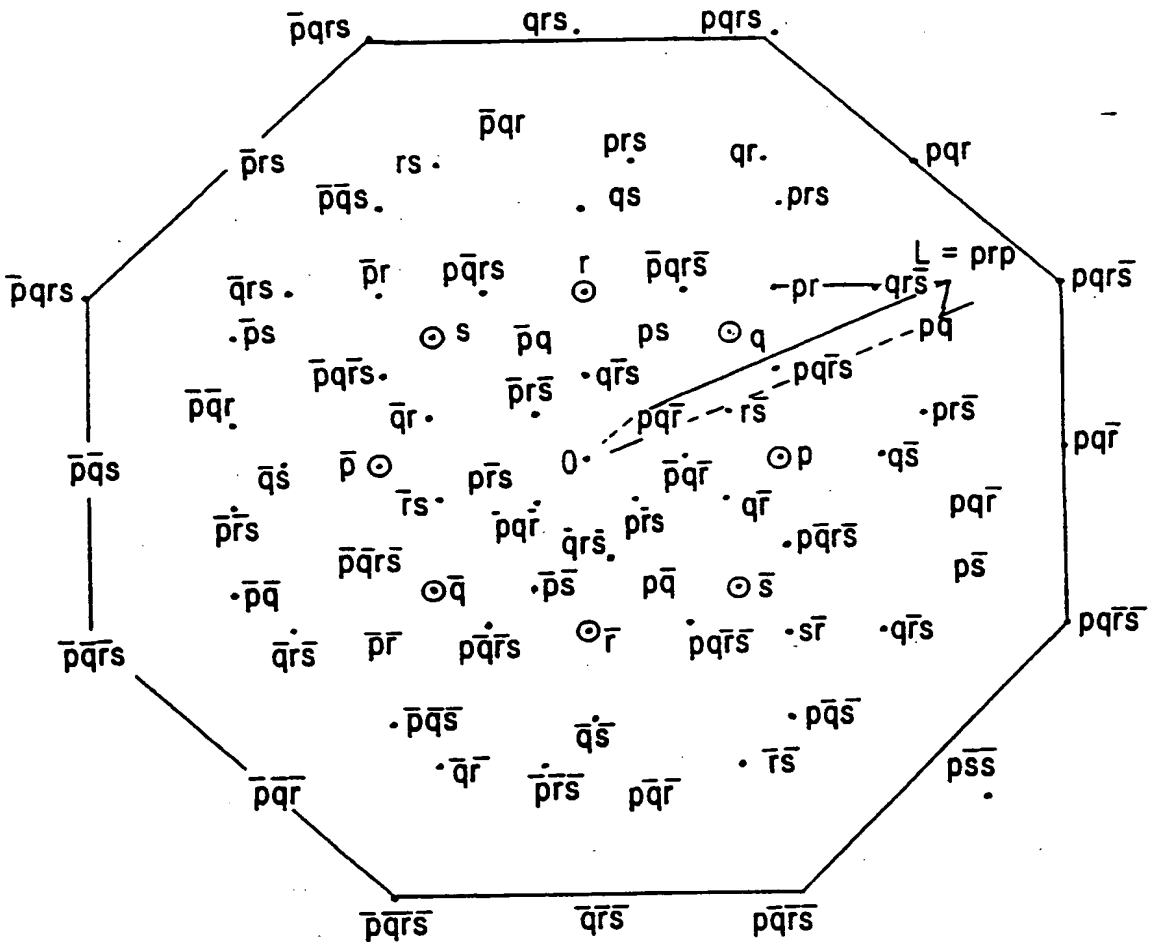


Figure 20

Undeveloped pq v pq̄r v p̄q̄r̄. . pq v pr v p̄q̄r̄

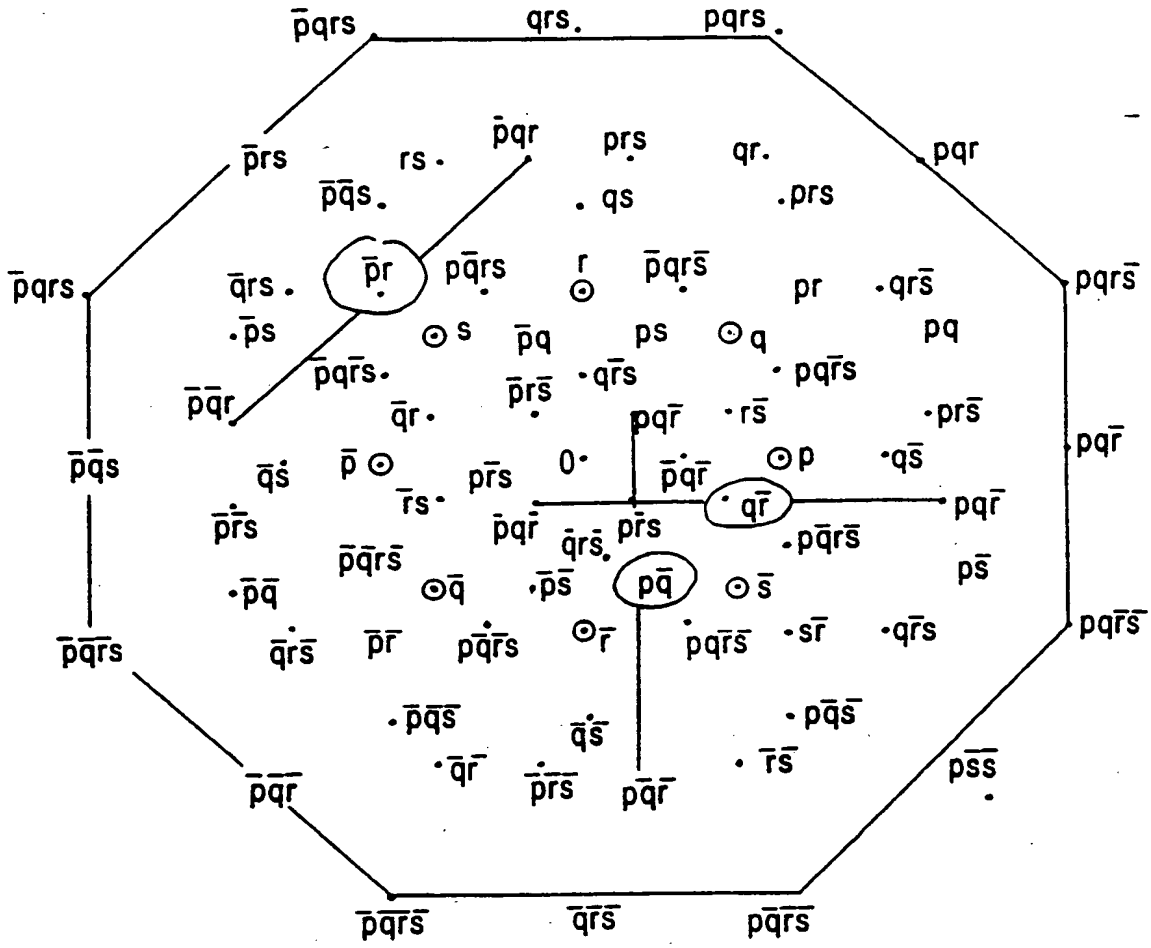


Figure 21

Simplification of Developed p̄q v pq̄ v q̄r v qr̄:
p̄qr v p̄q̄r v p̄qr̄ v pqr̄ v pq̄r̄ v pq̄r. ∴. pq̄ v p̄r v pr̄

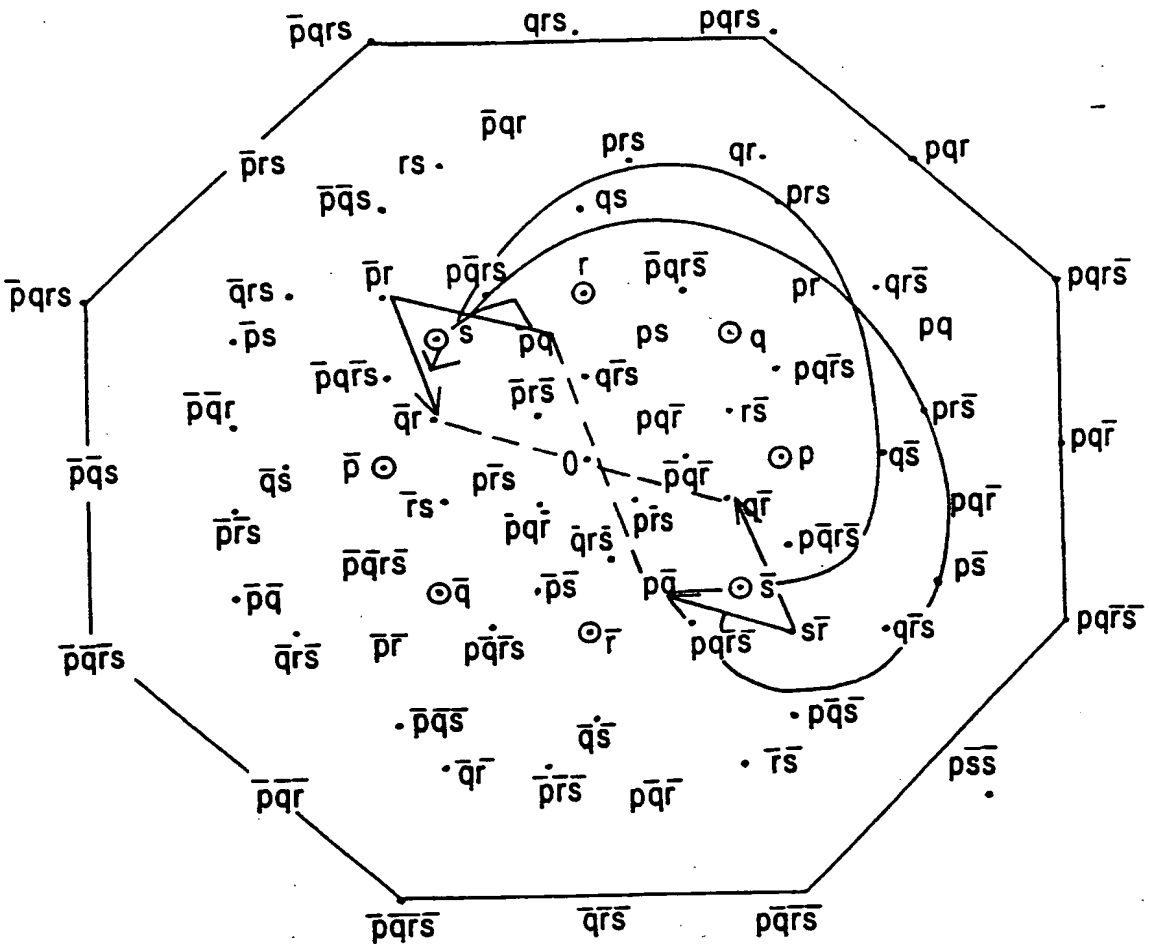


Figure 22

Simplification of Undeveloped p̄q v q̄r v pq̄ v qr̄

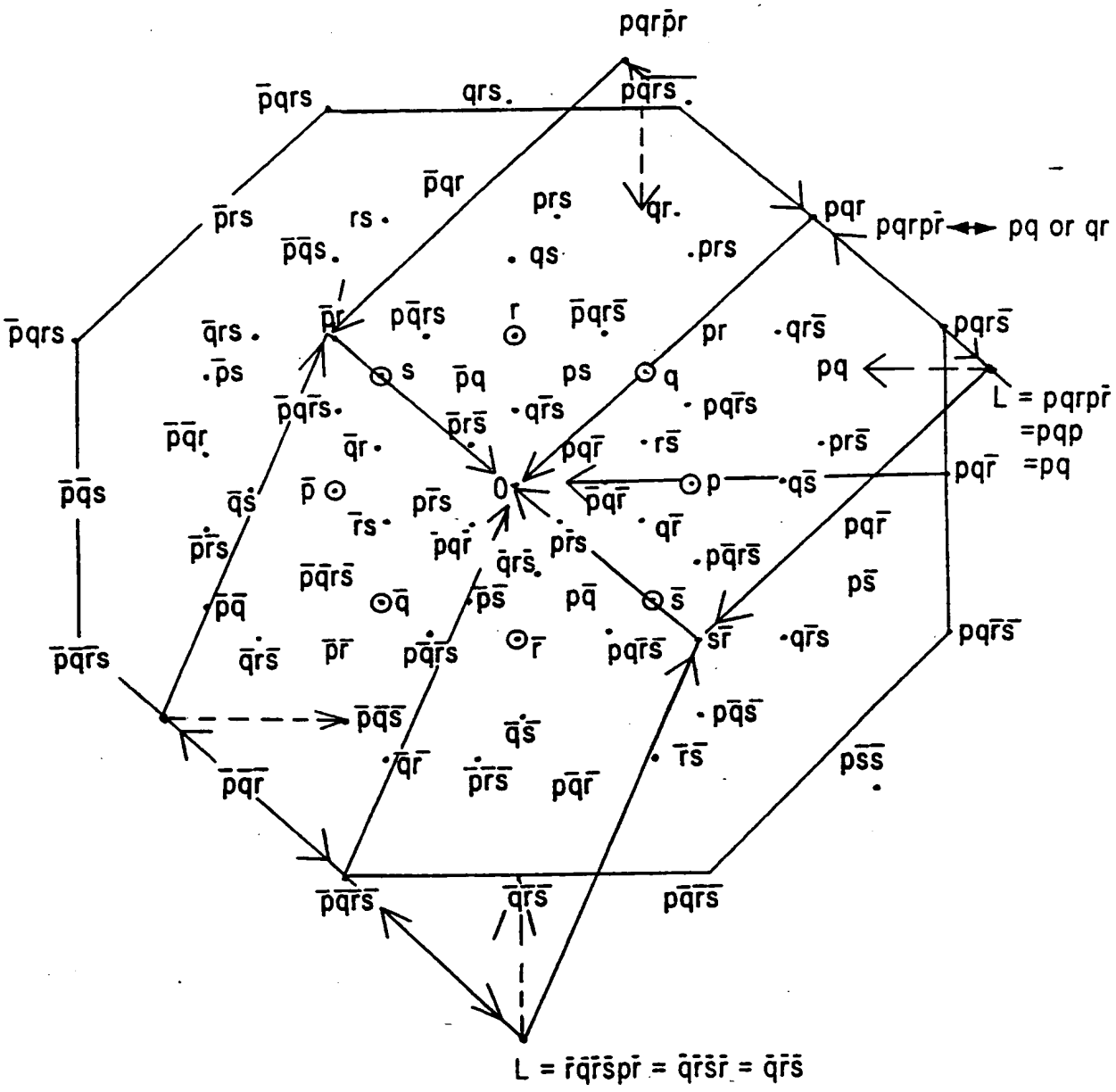


Figure 23

Simplification of pqr v pr̄ v pqs̄ v p̄r v p̄q̄r̄s̄

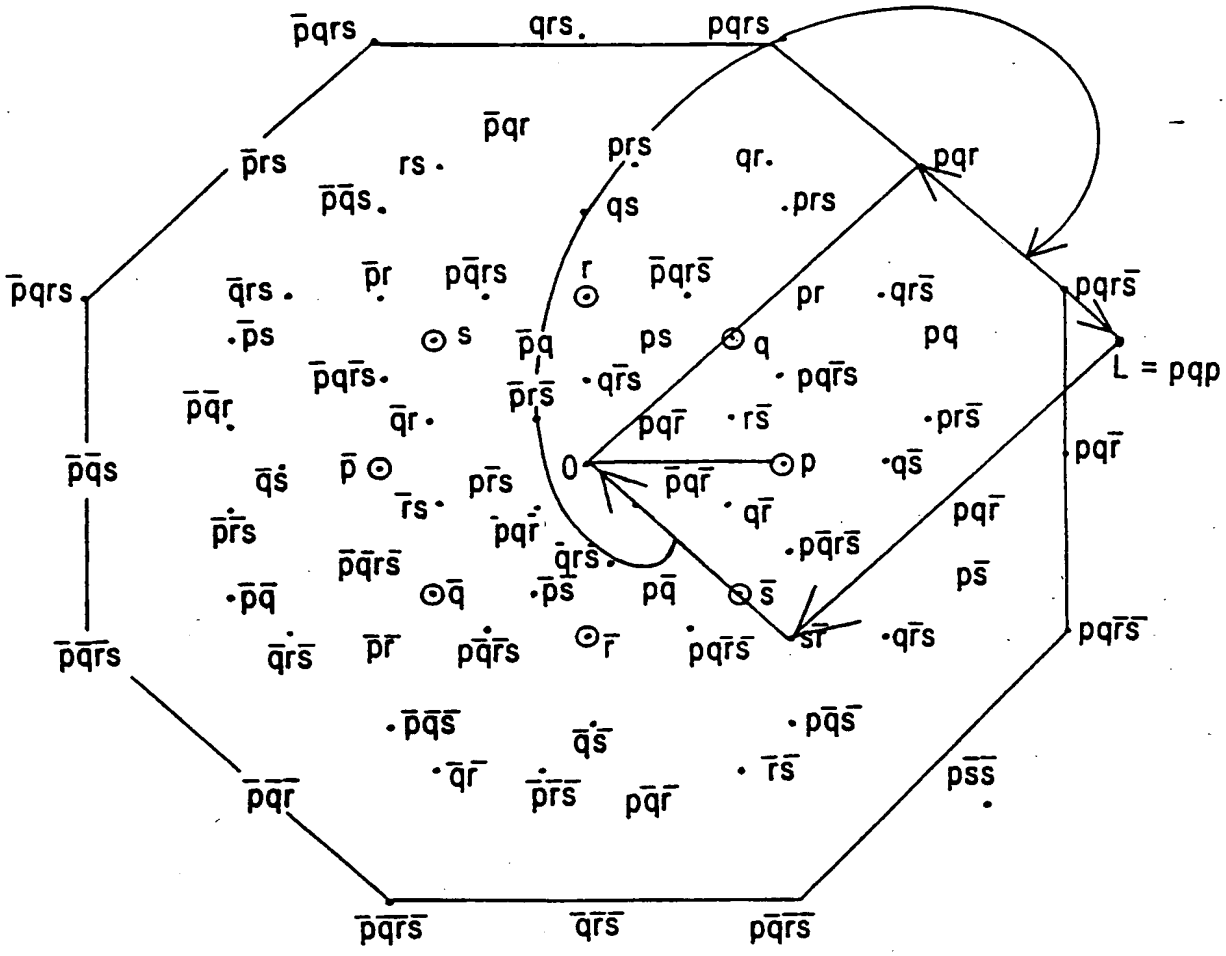


Figure 24

Equivalence of pqr and pq in pqr v pr̄

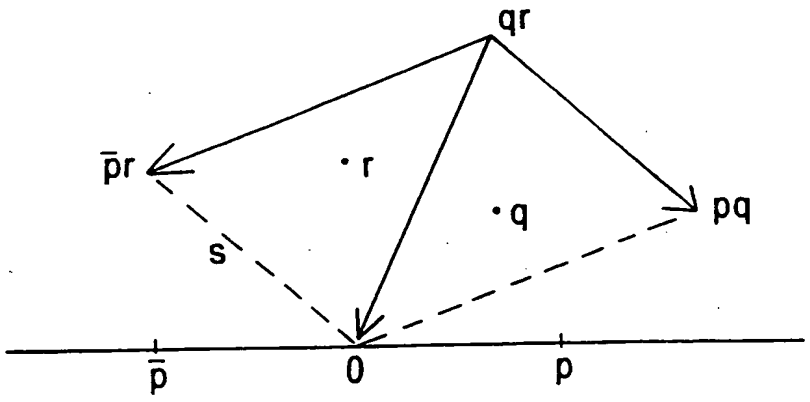


Figure 25
Consensus Theorem

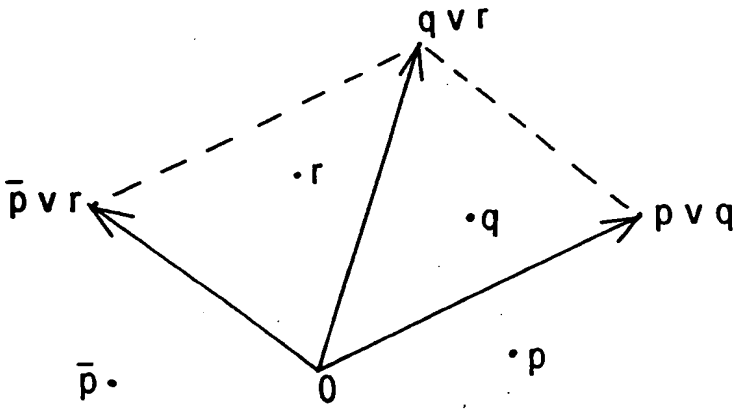


Figure 26
Consensus Theorem:
the Dual of qp v p̄r v qr is (q v p)(p̄ v r)(q v r)

p q̄ r	ANS qr v pq v p̄r	(q v p)	CNS (p̄ v r)	(q v r)
T T T	T T			
T T F	T		F	
T F T				
T F F			F	F
F T T	T	T		
F T F				
F F T		T	F	
F F F			F	F

Figure 24A

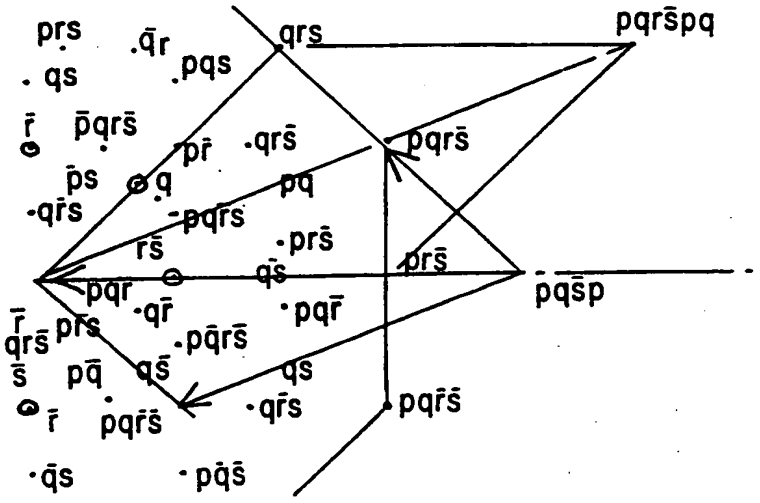


Figure 27

: Superfluity of pqs̄ in pqr v pr̄ v pqs̄

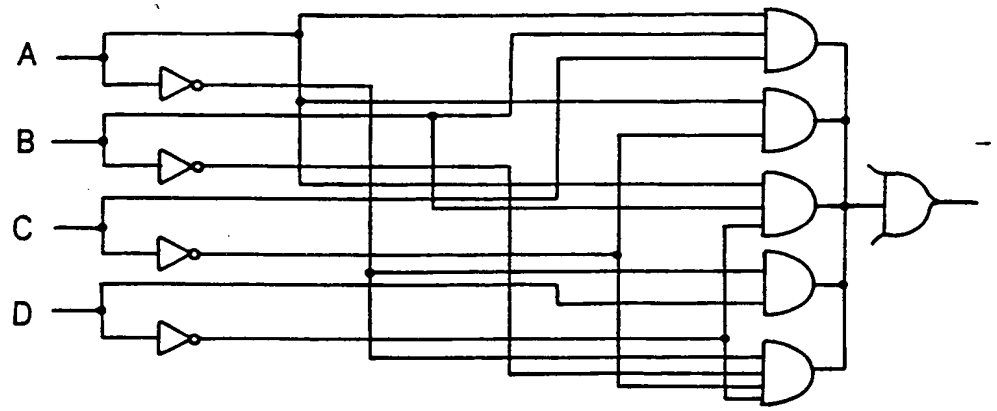


Figure 28

Target Circuit: $ABC + A\bar{C} + AB\bar{D} + \bar{A}C + \bar{A}\bar{B}\bar{C}\bar{D}$
G=5, I=12, R=7

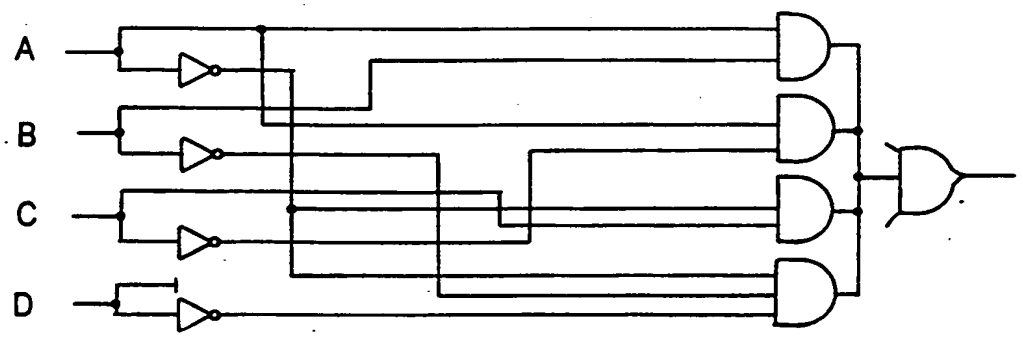


Figure 29

A Simplest Circuit Equivalent to the Target Circuit
$(ABC + A\bar{C} + ABD + \bar{A}C + \bar{A}\bar{B}\bar{C}\bar{D}) =$
$(AB + A\bar{C} + \bar{A}C + \bar{A}\bar{B}\bar{D})$
G=4, I=9, R=2

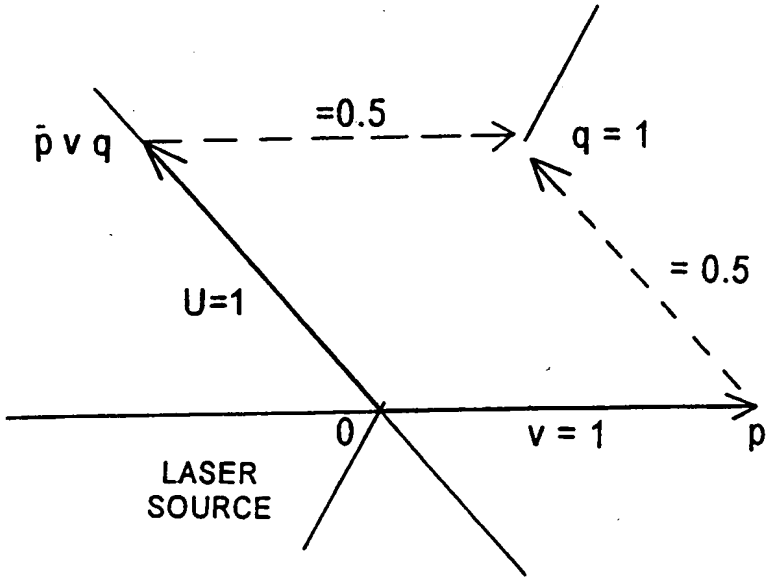


Figure 30

Optical Computation of modus ponens

Implication

Half-implication

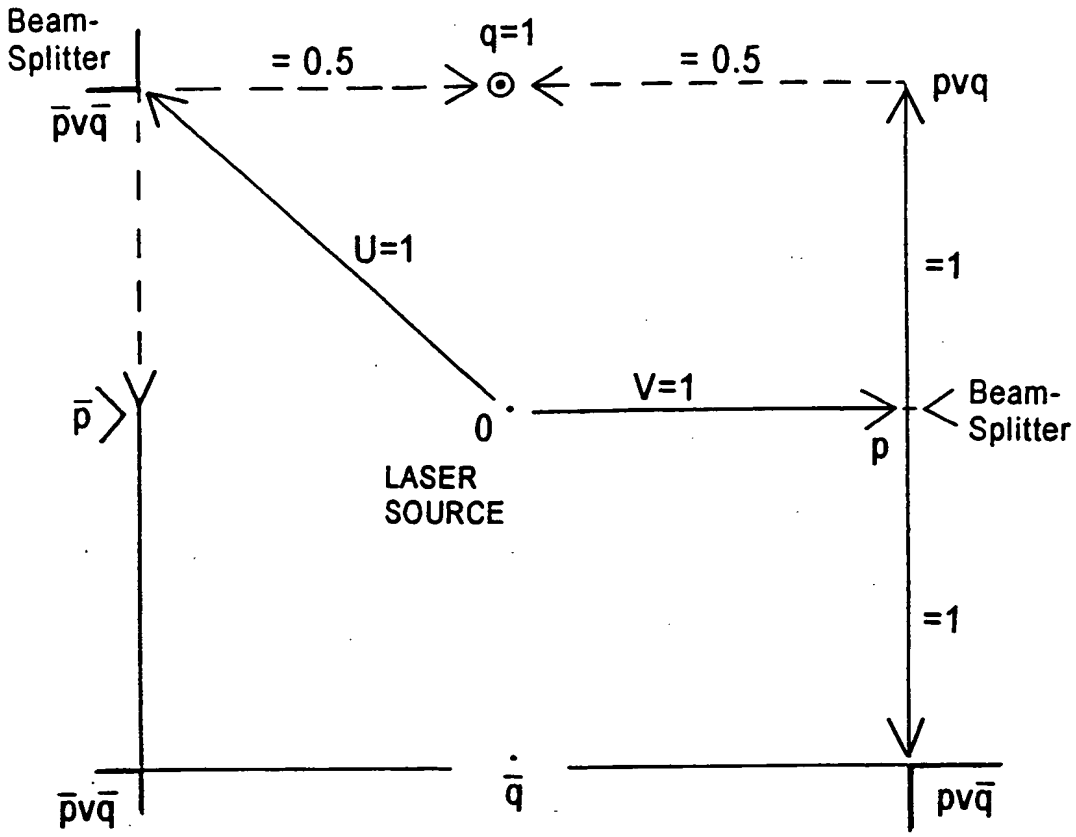


Figure 31
Interferometric Processing for modus ponens

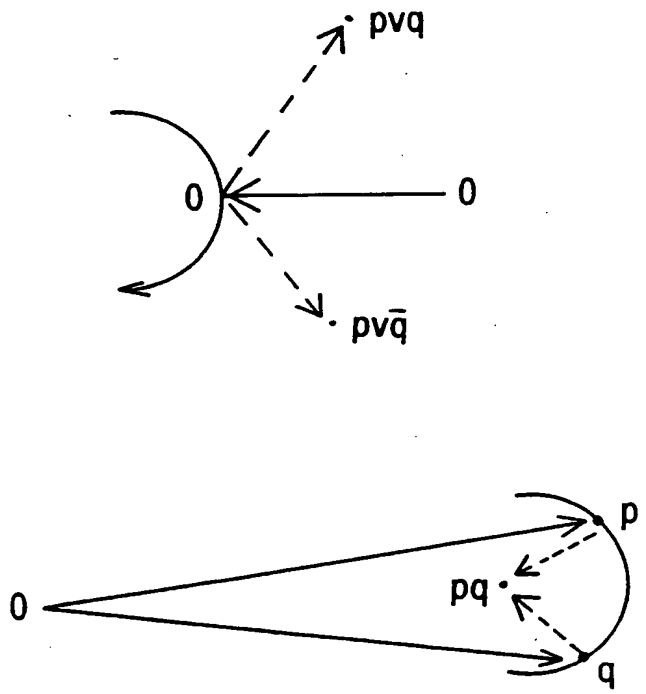


Figure 32

p and pq nodes in (p,q) space

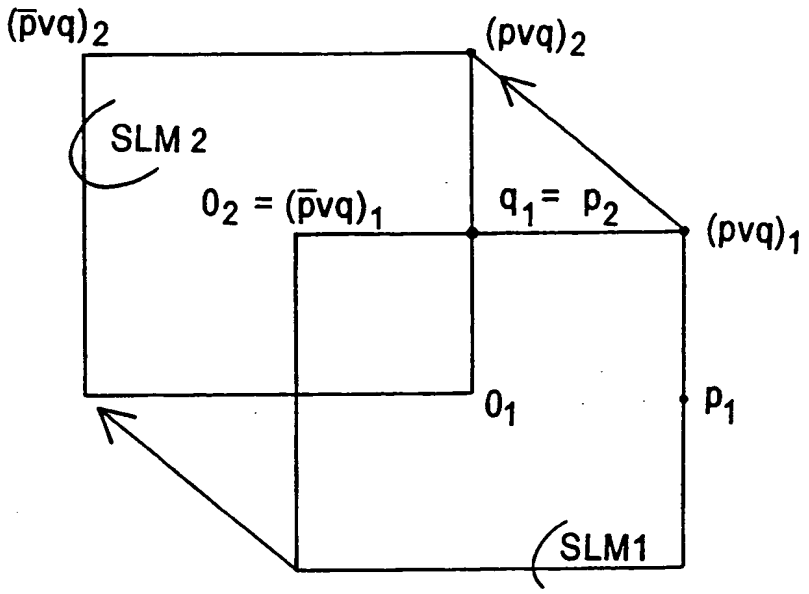


Figure 33
Displacement of O to $\bar{p}$ v q; p is q

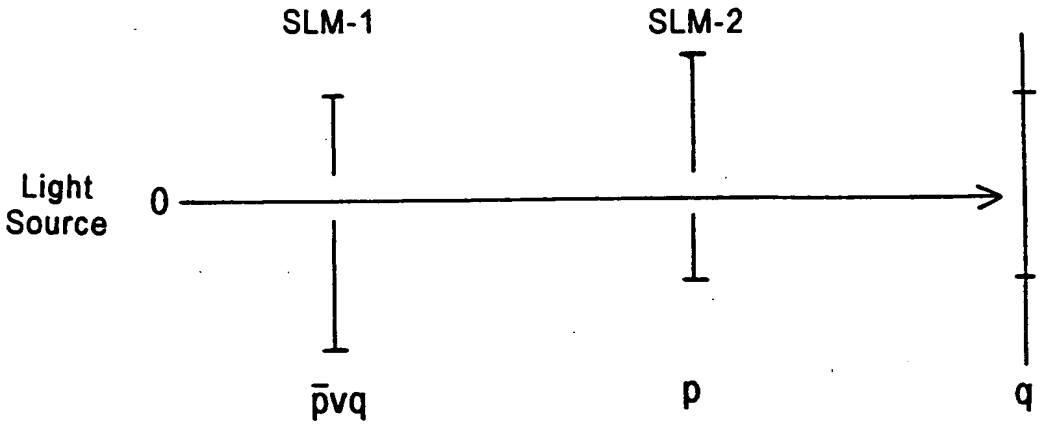


Figure 34

Vector Addition with Sequences of SLMs for modus ponens

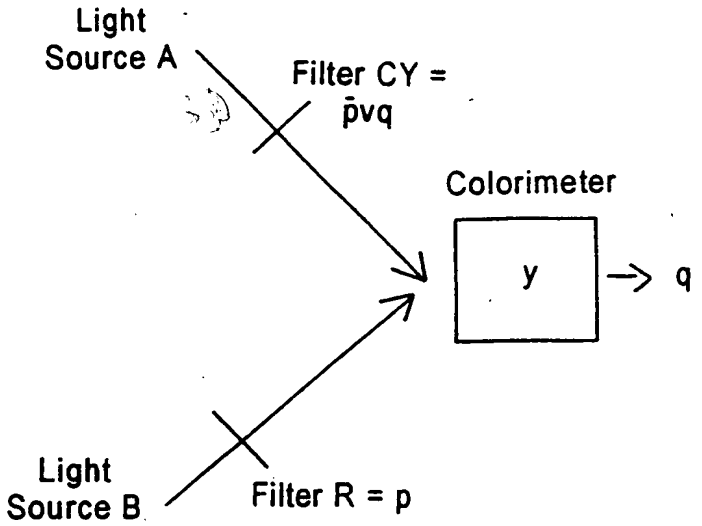


Figure 35

Colorimetric Computation of modus ponens

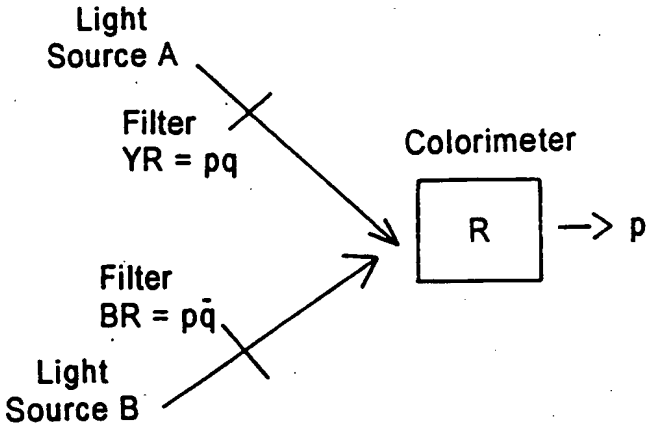


Figure 36

Colorimetric Simplification of pq v pq̄

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/21955

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 17/50
US CL :395/500.03, 500.18, 500.19, 500.23

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/500.02-500.19, 500.23, 500.34-500.37; 700/97, 117, 121

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

BRS (EAST), STN, DRLINK, IEE/IEEE
search terms: circuit$, logic$, simpli$, reduc$, vector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- A	US 5,649,165 A (JAIN et al) 15 July 1997, col. 8, lines 25-51; col. 10, line 34 to col. 15 line 27.	1-3, 5-12 --- 4
X — A	NGUYEN, T.V. et al. Multipoint Pade Approximation Using a Rational Block Lanczos Algorithm 1997 IEEE/ACM International Conference on Computer-Aided Design, 1997, Digest of Technical Papers. 09 November 1997. pages 72-74, sections 1-3.	1-3,5-12 --- 4
X,P --- A,P	US 5,920,484 A (NGUYEN et al) 06 July 1999, especially abstract; col. 1, lines 11-33; col. 3, line 10 to col. 6, line 38.	1-3, 5-12 --- 4

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
13 DECEMBER 1999

Date of mailing of the international search report
03 FEB 2000

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703) 305-3230

Authorized officer
Paul R. Lintz
Telephone No. (703) 305-3832

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/21955

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- A	US 5,640,328 A (LAM) 17 June 1997, especially Figures 1-2; col. 1, lines 14-67; col. 4, line 3 to col. 5, line 6.	1-3, 5-12 ---------- 4

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 17/50 | A1

(11) International Publication Number: **WO 00/17788**

(43) International Publication Date: 30 March 2000 (30.03.00)

(21) International Application Number: PCT/US99/21955

(22) International Filing Date: 22 September 1999 (22.09.99)

(30) Priority Data:
60/101,371 22 September 1998 (22.09.98) US

(71)(72) Applicant and Inventor: WESTPHAL, Jonathan [US/US]; 7620 Valley Vista Road, Pocatello, ID 83201 (US).

(74) Agents: STEWART, David, L. et al.; McDermott, Will & Emery, 600 13th Street, N.W., Washington, DC 20005-3096 (US).

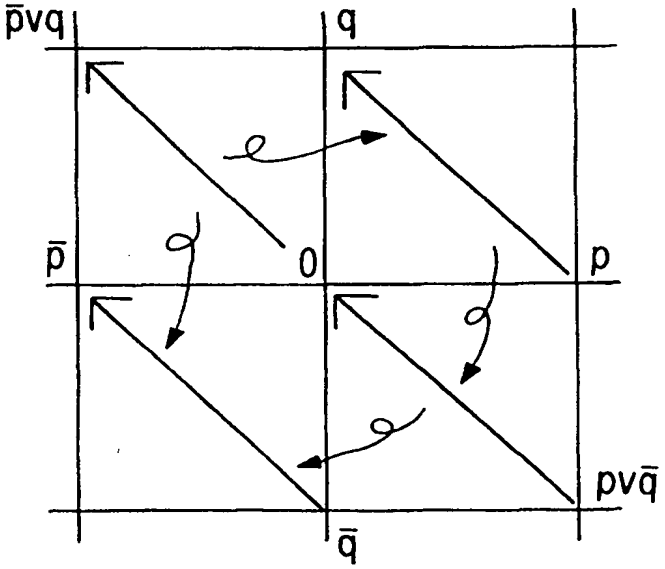
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DEVICES AND TECHNIQUES FOR LOGICAL PROCESSING

(57) Abstract

The invention is directed to apparatus, methods, systems and computer program products which permit a simplification of the logic required for performing a certain function to a minimum set of logical elements of operations, permitting a complex digital circuitry to be simplified so that the processing speed for performing the complex digital operations, is reduced. This is accomplished by using a system of propositional logic (13B), representing the logic of a logical circuit to be designed as points and vectors in a vector space, simplifying the logic of the logical circuit to a simpler form using the points and vectors in a vector space, and designing the circuit using the simpler form.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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EE	Estonia	**LR**	Liberia	**SG**	Singapore		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/21955

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 17/50
US CL :395/500.03, 500.18, 500.19, 500.23
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/500.02-500.19, 500.23, 500.34-500.37; 700/97, 117, 121

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

BRS (EAST), STN, DRLINK, IEE/IEEE
search terms: circuit$, logic$, simpli$, reduc$, vector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- A	US 5,649,165 A (JAIN et al) 15 July 1997, col. 8, lines 25-51; col. 10, line 34 to col. 15 line 27.	1-3, 5-12 --- 4
X -- A	NGUYEN, T.V. et al. Multipoint Pade Approximation Using a Rational Block Lanczos Algorithm 1997 IEEE/ACM International Conference on Computer-Aided Design, 1997, Digest of Technical Papers. 09 November 1997. pages 72-74, sections 1-3.	1-3,5-12 --- 4
X,P ---- A,P	US 5,920,484 A (NGUYEN et al) 06 July 1999, especially abstract; col. 1, lines 11-33; col. 3, line 10 to col. 6, line 38.	1-3, 5-12 --- 4

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 13 DECEMBER 1999	Date of mailing of the international search report 03 FEB 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Paul R. Lintz James R. Matthews Telephone No. (703) 305-3832

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/21955

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- A	US 5,640,328 A (LAM) 17 June 1997, especially Figures 1-2; col. 1, lines 14-67; col. 4, line 3 to col. 5, line 6.	1-3, 5-12 ---------- 4

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To: DAVID L. STEWART
MCDERMOTT, WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)* 20 DEC 2000	
Applicant's or agent's file reference 52254-013	IMPORTANT NOTIFICATION

International application No.	International filing date *(day/month/year)*	Priority Date *(day/month/year)*
PCT/US99/21955	22 SEPTEMBER 1999	22 SEPTEMBER 1998

Applicant
WESTPHAL, JONATHAN

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer MATTHEW S. SMITH
Facsimile No. (703) 305-3230	Telephone No. (703) 308-1323

Form PCT/IPEA/416 (July 1992)*

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 52254-013	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US99/21955	International filing date *(day/month/year)* 22 SEPTEMBER 1999	Priority date *(day/month/year)* 22 SEPTEMBER 1998
International Patent Classification (IPC) or national classification and IPC IPC(7): G06F 17/50 and US Cl.: 716/3, 17, 18; 703/2		
Applicant WESTPHAL, JONATHAN		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 7 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 9 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report

   II ☐ Priority

   III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability

   IV ☐ Lack of unity of invention

   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   VI ☒ Certain documents cited

   VII ☒ Certain defects in the international application

   VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
19 APRIL 2000	28 NOVEMBER 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MATTHEW S. SMITH Telephone No. (703) 308-1323

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/21955

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-26 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the claims:
pages 27-29 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the drawings:
pages 1-34 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

[X] the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages NONE

[X] the claims, Nos. NONE

[X] the drawings, sheets~~/fig~~ NONE

5. [ ] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	4	YES
	Claims	1-3,5-12	NO
Inventive Step (IS)	Claims	4	YES
	Claims	1-3,5-12	NO
Industrial Applicability (IA)	Claims	1-12	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **JAIN et al.** (US Patent No. 5,649,165).

JAIN et al. disclose a computer-aided design system and method for performing logic design analysis for determining logical interdependencies between points in a digital circuit topology by using points and vectors for boolean circuit representation in the BDD simplification (abstract; Fig. 2).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are summarized in col. 8, lines 25-51, wherein the use of points and vectors space to simplify the circuit (i.e., points and vectors associated BDD simplification) is further described in col. 11, line 16 to col. 15, line 27, and since the method of **JAIN et al.** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **LAM** (US Patent No. 5,640,328).

LAM discloses a method and apparatus for determining the location of electric leaf cell circuits within the architecture of a semiconductor chip which includes determination of the longest signal delays through an electric leaf cell circuit by evaluating independent channel connect components, reorganizing the circuit elements of each channel under evaluation into acyclic form, restructuring the acyclic form of channel connected components within the electric leaf cell circuits being structurally positioned in the chip architecture by selected reduction processes, determining input state vectors for each input and output pin connection pair of the electric leaf cell circuit in which an input pin connection state change is reflected in an output connection (Continued on Supplemental Sheet.)

VI. Certain documents cited

1. Certain published documents (Rule 70.10)

Application No. Patent No.	Publication Date *(day/month/year)*	Filing Date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*
US, A, 6,041,170	21 MARCH 2000	31 JULY 1997	NONE
US, A, 6,023,573	08 FEBRUARY 2000	29 JANUARY 1999	01 SEPTEMBER 1998

2. Non-written disclosures (Rule 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

Claim 4 is objected to under PCT Rule 66.2(a)(iii) as containing the following defect(s) in the form or contents thereof: the semicolon ";" after "zero" and the period "." in step (f1) should be comma "," and semicolon ";" respectively; the period in step (g1) should be comma ",".

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim 4 is objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because the claim is indefinite for the following reason(s): step (g1) refers to the content in "Figure 14" rendering the claim omnibus and "then 6" lacks antecedent basis, and step (h1) containing "(i.e., if all equivalences in the system have been exploited)" is improperly defined.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):
pin state change, and determining placement of the leaf cell within a semiconductor circuit module with reference to the greatest delay within each leaf cell (abstract).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are illustrated in Figs. 1-2, wherein the use of points and vectors space to simplify the circuit (i.e., points and vectors associated BDD simplification) is further described in col. 4, line 3 to col. 5, line 6, and since the method of **LAM** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **NGUYEN, T. V. et al.** ("Multipoint Pade Approximation Using a Rational Block Lanczos Algorithm", 1997 IEEE/ACM International Conference on Computer-Aided Design, 1997, Digest of Technical Papers, 09 November 1997, pages 72-74).

NGUYEN, T. V. et al. disclose a multipoint Pade approximation using a rational block Lanzos algorithm to model/design circuits in digital, analog, or mixed signal designs (abstract).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are described in sections 1-3, wherein the rational block Lanczos algorithm provides for the simplification of circuit design using points and vectors space to simplify the circuit, and since the method of **NGUYEN, T. V. et al.** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claim 4 meets the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest one process rule of a set of process rules as claimed.

Claims 1-12 meet the criteria set out in PCT Article 33(4), Industrial Applicability, because the invention can be used in industry.

---------- NEW CITATIONS ----------
NONE

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner f r Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 29 May 2000 (29.05.00)	
International application No. PCT/US99/21955	**Applicant's or agent's file reference** 52254-013
International filing date (day/month/year) 22 September 1999 (22.09.99)	**Priority date** (day/month/year) 22 September 1998 (22.09.98)
Applicant WESTPHAL, Jonathan	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

19 April 2000 (19.04.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No.: (41-22) 740.14.35	Authorized officer Pascal Piri u Telephone No.: (41-22) 338.83.38

ATENT COOPERATION TRE. .TY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING SUBMISSION OR TRANSMITTAL OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

STEWART, David, L.
McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096
ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year) 15 May 2000 (15.05.00)	
Applicant's or agent's file reference 52254-013	**IMPORTANT NOTIFICATION**
International application No. PCT/US99/21955	International filing date (day/month/year) 22 September 1999 (22.09.99)
International publication date (day/month/year) 30 March 2000 (30.03.00)	Priority date (day/month/year) 22 September 1998 (22.09.98)
Applicant WESTPHAL, Jonathan	

1. The applicant is hereby notified of the date of receipt (except where the letters "NR" appear in the right-hand column) by the International Bureau of the priority document(s) relating to the earlier application(s) indicated below. Unless otherwise indicated by an asterisk appearing next to a date of receipt, or by the letters "NR", in the right-hand column, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. This updates and replaces any previously issued notification concerning submission or transmittal of priority documents.

3. An **asterisk(*)** appearing next to a date of receipt, in the right-hand column, denotes a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b). In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

4. The **letters "NR"** appearing in the right-hand column denote a priority document which was not received by the International Bureau or which the applicant did not request the receiving Office to prepare and transmit to the International Bureau, as provided by Rule 17.1(a) or (b), respectively. In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
22 Sept 1998 (22.09.98)	60/101,371	US	25 Apri 2000 (25.04.00)

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer

Dominique DELMAS

Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

To:

STEWART, David, L.
McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096
ETATS-UNIS D'AMERIQUE

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

Date of mailing (day/month/year) 28 June 2000 (28.06.00)	
Applicant's or agent's file reference 52254-013	**IMPORTANT NOTIFICATION**
International application No. PCT/US99/21955	**International filing date** (day/month/year) 22 September 1999 (22.09.99)

1. The following indications appeared on record concerning:

[X] the applicant [ ] the inventor [ ] the agent [ ] the common representative

Name and Address	State of Nationality	State of Residence
WESTPHAL, Jonathan 7620 Valley Vista Road Pocatello, ID 83201 United States of America	US	US
	Telephone No.	
	Facsimile No.	
	Teleprinter No.	

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[X] the person [X] the name [ ] the address [ ] the nationality [ ] the residence

Name and Address	State of Nationality	State of Residence
VECTORLOG 7620 Valley Vista Road Pocatello, ID 83201 United States of America	US	US
	Telephone No.	
	Facsimile No.	
	Teleprinter No.	

3. Further observations, if necessary:
The above-mentioned inventor is to be considered as applicant/inventor for the purposes of the United States of America only, since he assigned his rights for all designated States except US to a new applicant as indicated below.

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[X] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland** Facsimile No.: (41-22) 740.14.35	Authorized officer Dominique DELMAS Telephone No.: (41-22) 338.83.38

Form PCT/IB/306 (March 1994)

003378367

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

To:
STEWART, David, L.
McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096
ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year) 30 March 2000 (30.03.00)	
Applicant's or agent's file reference 52254-013	**IMPORTANT NOTICE**
International application No. PCT/US99/21955	**International filing date** (day/month/year) 22 September 1999 (22.09.99)
Priority date (day/month/year) 22 September 1998 (22.09.98)	
Applicant WESTPHAL, Jonathan	

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   AU,CN,JP,KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   AE,AL,AM,AP,AT,AZ,BA,BB,BG,BR,BY,CA,CH,CR,CZ,DE,DK,DM,EA,EE,EP,ES,FI,GB,GD,GE,GH,
   GM,HR,HU,ID,IL,IN,IS,KE,KG,KZ,LC,LK,LR,LS,LT,LU,LV,MD,MG,MK,MN,MW,MX,NO,NZ,OA,PL,
   PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,TZ,UA,UG,UZ,VN,YU,ZA,ZW
   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   30 March 2000 (30.03.00) under No. WO 00/17788

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer
J. Zahra

Telephone No. (41-22) 338.83.38

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

REC'D 27 DEC 2000
WIPO PCT

Applicant's or agent's file reference 52254-013	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US99/21955	International filing date *(day/month/year)* 22 SEPTEMBER 1999	Priority date *(day/month/year)* 22 SEPTEMBER 1998
International Patent Classification (IPC) or national classification and IPC IPC(7): G06F 17/50 and US Cl.: 716/3, 17, 18; 703/2		
Applicant WESTPHAL, JONATHAN		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority. (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 0 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☒ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
19 APRIL 2000	28 NOVEMBER 2000
Name and mailing address of the IPEA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MATTHEW S. SMITH Telephone No. (703) 308-1323

Form PCT/IPEA/409 (cover sheet) (July 1998)★

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/21955

I. Basis of the report

1. With regard to the **elements** of the international application:*

[X] the international application as originally filed

[X] the description:
pages 1-26 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of

[X] the claims:
pages 27-29 , as originally filed
pages NONE , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of

[X] the drawings:
pages 1-34 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of

[X] the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

[ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

[ ] the language of publication of the international application (under Rule 48.3(b)).

[ ] the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

[ ] contained in the international application in printed form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readable form.

[ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] The statement that the information recorded in computer readable form is identical to the writen sequence listing has been furnished.

4. [X] The amendments have resulted in the cancellation of:

[X] the description, pages NONE

[X] the claims, Nos. NONE

[X] the drawings, sheets/~~fig~~ NONE

5. [ ] This report has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

***Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/21955

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	4	YES
	Claims	1-3,5-12	NO
Inventive Step (IS)	Claims	4	YES
	Claims	1-3,5-12	NO
Industrial Applicability (IA)	Claims	1-12	YES
	Claims	NONE	NO

2. citations and explanations (Rule 70.7)

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **JAIN et al.** (US Patent No. 5,649,165).

JAIN et al. disclose a computer-aided design system and method for performing logic design analysis for determining logical interdependencies between points in a digital circuit topology by using points and vectors for boolean circuit representation in the BDD simplification (abstract; Fig. 2).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are summarized in col. 8, lines 25-51, wherein the use of points and vectors space to simplify the circuit (i.e., points and vectors associated BDD simplification) is further described in col. 11, line 16 to col. 15, line 27, and since the method of **JAIN et al.** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **LAM** (US Patent No. 5,640,328).

LAM discloses a method and apparatus for determining the location of electric leaf cell circuits within the architecture of a semiconductor chip which includes determination of the longest signal delays through an electric leaf cell circuit by evaluating independent channel connect components, reorganizing the circuit elements of each channel under evaluation into acyclic form, restructuring the acyclic form of channel connected components within the electric leaf cell circuits being structurally positioned in the chip architecture by selected reduction processes, determining input state vectors for each input and output pin connection pair of the electric leaf cell circuit in which an input pin connection state change is reflected in an output connection (Continued on Supplemental Sheet.)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US99/21955

VI. Certain documents cited

1. Certain published documents (Rule 70.10)

Application No. Patent No.	Publication Date *(day/month/year)*	Filing Date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*
US, A, 6,041,170	21 MARCH 2000	31 JULY 1997	NONE
US, A, 6,023,573	08 FEBRUARY 2000	29 JANUARY 1999	01 SEPTEMBER 1998

2. Non-written disclosures (Rule 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

Claim 4 is objected to under PCT Rule 66.2(a)(iii) as containing the following defect(s) in the form or contents thereof: the semicolon ";" after "zero" and the period "." in step (f1) should be comma "," and semicolon ";" respectively; the period in step (g1) should be comma ",".

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim 4 is objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because the claim is indefinite for the following reason(s): step (g1) refers to the content in "Figure 14" rendering the claim omnibus and "then 6" lacks antecedent basis, and step (h1) containing "(i.e., if all equivalences in the system have been exploited)" is improperly defined.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):
pin state change, and determining placement of the leaf cell within a semiconductor circuit module with reference to the greatest delay within each leaf cell (abstract).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are illustrated in Figs. 1-2, wherein the use of points and vectors space to simplify the circuit (i.e., points and vectors associated BDD simplification) is further described in col. 4, line 3 to col. 5, line 6, and since the method of **LAM** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claims 1-3,5-12 lack novelty under PCT Article 33(2) as being anticipated by **NGUYEN, T. V. et al.** ("Multipoint Pade Approximation Using a Rational Block Lanczos Algorithm", 1997 IEEE/ACM International Conference on Computer-Aided Design, 1997, Digest of Technical Papers, 09 November 1997, pages 72-74).

NGUYEN, T. V. et al. disclose a multipoint Pade approximation using a rational block Lanzos algorithm to model/design circuits in digital, analog, or mixed signal designs (abstract).

As per **claims 1-3,5-12**, the steps/means/apparatus of representing the logic of a logical circuit to be design as points and vectors in a vector space; using the points and vectors in a vector space to simplify the logic of the logic circuit to a simplier form; and designing/implementing the logical circuit using the simpler form are described in sections 1-3, wherein the rational block Lanczos algorithm provides for the simplification of circuit design using points and vectors space to simplify the circuit, and since the method of **NGUYEN, T. V. et al.** is computer-aided design, the memory, program, processing element including optical computer, digital computer, colorimetric computer, and analog computer are inherently included, as is well known in the art.

Claim 4 meets the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest one process rule of a set of process rules as claimed.

Claims 1-12 meet the criteria set out in PCT Article 33(4), Industrial Applicability, because the invention can be used in industry.

---------- NEW CITATIONS ----------
NONE